Application Report
SLAA301–July 2006

Using TDM Function to Interface Four TLV320AIC33 Codecs With a Single Host Processor

Wendy Fang — *DAP - Industrial Audio*

ABSTRACT

This application report discusses how to use the TLV320AIC33 audio data port's time-division multiplexing (TDM) function to connect, interface, and run four TLV320AIC33 codec devices simultaneously under the control of a single host processor. Four TLV320AIC33 EVM boards and one USB-MODEVM board were used to test the interface and function.

Contents

List of Figures

List of Tables

1 Introduction

To use a TLV320AIC33 (or AIC33 for short) codec device, the host processor or DSP needs two digital serial buses to communicate with the codec (see SLAS480). The two buses are:

- The control interface (I^2C or SPI bus) to set up and control the codec
- The audio data interface (I^2S bus) to transfer audio data between the host and the codec

With some applications, more than one AIC33 codec can be used and controlled by a single host processor. A multiple AIC33 system saves resources and simplifies the whole system. Figure 1 shows a block diagram of such a system.

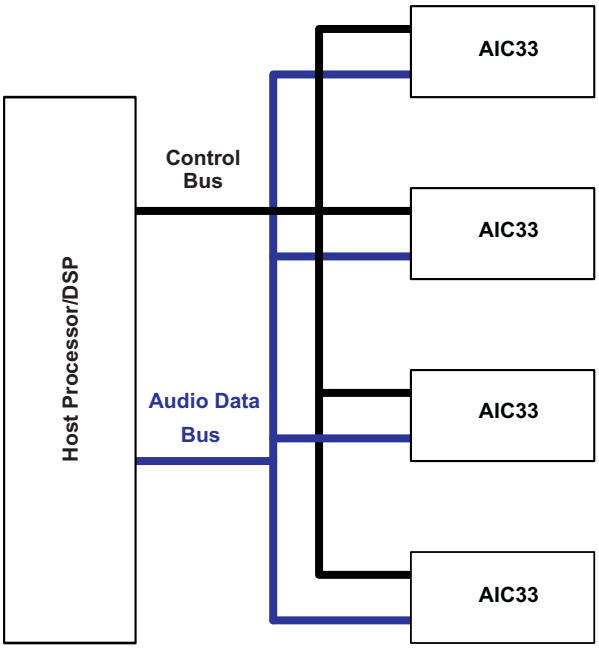


Figure 1. Four AIC33 Codecs Interfaced With a Single Host Processor/DSP

This application report discusses how to set up, configure, connect, and run the system shown in Figure 1. The system has been tested using four TI AIC33 EVM boards and one TI USB-MODEVM board. One AIC33 codec is on each of the EVM boards; the host processor (a TI TAS1020B USB controller) is located on the USB-MODEVM board. See the SBAU114 user's guide for details on the AIC33EVM and AIC33EVM-PDK.

2 Considerations

To implement the system shown in Figure 1, a host processor and four AIC33 devices are needed. This application report used one USB-MODEVM board and four AIC33EVM boards. The USB-MODEVM board is not individually orderable but is a part of TLV320AIC33EVM-PDK. Thus, to duplicate this application, the user needs to order three TLV320AIC33EVM, and one TLV320AIC33EVM-PDK that includes one TLV320AIC33EVM board and one USB-MODEVM board.

Certain steps are critical for setting up and running a four-AIC33 codec system. This section of this application report focuses on additional operation limitations or considerations for stacking four AIC33 EVMs to implement and operate the system shown in Figure 1.

2.1 Power Supply

During power up, the motherboard (USB-MODEVM) can draw about 100 mA by itself. During operation, the USB-MODEVM plus one AIC33 can require current of 200 mA or more. Therefore, it can be expected that the system shown in Figure 1 will require much higher current than 200 mA.

The current budget on a full-rated USB port can be a maximum of 500 mA. Thus, to operate the four

AIC33EVM stacking system through a power supply from the USB cable (connected to the USB-MODEVM board) may be questionable. However, as discussed in this application report, because not more than two of the same audio outputs from different AIC33 devices should be enabled simultaneously, it may be acceptable to use the USB power supply for the four AIC33EVMs stacking operation.

For safety, however, it is recommended to use a laboratory power supply for powering and testing the four AIC33EVM stacked system.

To connect power from an external laboratory power supply, move JMP6 to 2~3 on the USB-MODEVM board, and then connect the laboratory power supply, ranging from 6 Vdc to 10 Vdc, to the board through the J8 terminal block or J9 power connector. See the section on USB-MODEVM Interface Power in the user's guide SBAU114 for more details.

2.2 Digital Connections

The digital pins on an AIC33 device includes the control bus pins (SPI or I^2C); the audio data bus pins (I^2S or DSP or other); and other GPIO pins, such as GPIO1 or MFP2.

All of these digital signals are available on an AIC33EVM board through the board's J16 and J17 connectors.

2.2.1 Control Interface

To operate four AIC33 codecs together, only the I^2C bus (not the SPI) should be used as the control interface.

Before stacking an AIC33EVM on top of the USB-MODEVM, the following hardware jumpers on the AIC33EVM board need to be set up:

- Wire the AIC33 devices' SELECT pin *low* (set JMP10 to 3~5 on the AIC33 EVM boards)
- Set the address pins (A1 and A0) on the four AIC33 devices differently. That is, set up JMP11 and JMP12 as shown in Table 1:

Table 1. I^2C Address Settings

JMP12	JMP11	A1	A0
3~5	3~5	0	0
3~5	1~3	0	1
1~3	3~5	1	0
1~3	1~3	1	1

2.2.2 Audio Data Interface

On the AIC33EVM-PDK system, the AIC33 audio data is streamed, between the system and a PC, through the onboard TAS1020B processor on the USB-MODEVM board. The firmware on the TAS1020B processor cannot work in TDM mode. Thus, an external host processor is needed to interface with these AIC33 devices as the audio data bus master; or one of the AIC33 should be configured as the audio data bus master.

This application report applied the first AIC33 as the audio interface master; and the rest of the AIC33s are slaves.

The steps to configure the audio interface include:

1. Disable the onboard I^2S from the TAS1020B by turning OFF SW2-4 on the USB-MODEVM board.
2. Configure all AIC33 codecs to the device's DSP + TDM mode and with different offset bits, so as to share the single audio interface bus within the four AIC33 devices. That is:
   - Set D5 in Page0/Reg8 to 1 (DOUT should be in 3-state mode when valid data is not being sent);
   - Set D7-D6 in Page0/Reg9 to 01 (serial data bus uses DSP mode);
   - Set Page0/Reg10 corresponding to the location of the particular AIC33EVM board and the

data word length. For example: if the *Word Length* = 2x16-bit (for both left and right channels) in the interface, set the register at each AIC33 according to Table 2:

Table 2. TDM Bus Different Bit Delay on Four AIC33EVMs (Under the 16-Bit Word Length)

Device No.	A1 A0	Page0/Reg10 Setting	Description
AIC33#0	00	0x00	Data Offset = 0-bit clocks
AIC33#1	01	0x20	Data Offset = 32-bit clocks
AIC33#2	10	0x40	Data Offset = 64-bit clocks
AIC33#3	11	0x60	Data Offset = 96-bit clocks

Figure 2 shows the timing of the TDM bus's bit clock, BCLK, where the system connection is the same as is shown in Figure 1 and the offsets of the four AIC33 devices are set up as shown in Table 2.

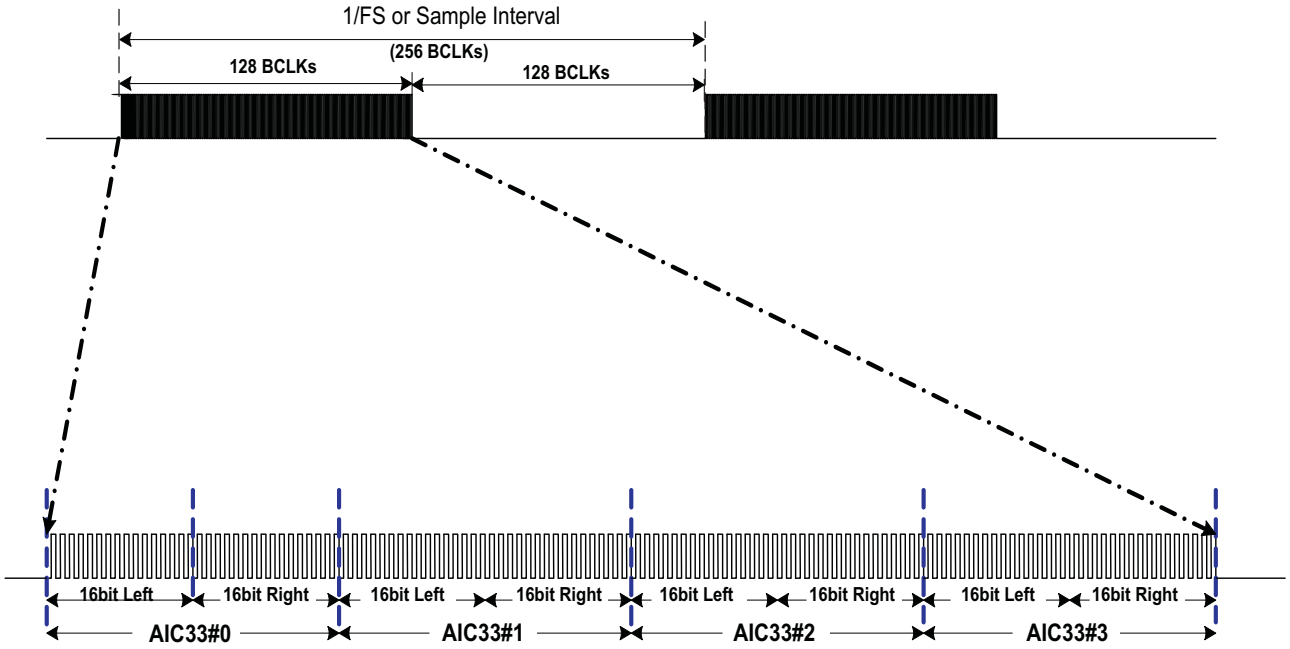


Figure 2. BCLKs for Four AIC33 Slots

2.2.3 Other Digital GPIOs

All other digital pins, including GPIO0, GPIO1, MFP2, and MFP3, must be kept in a 3-state mode with four stacked AIC33 EVMs. That is, they should be left at their power-up default condition.

2.3 Analog Connections

All the AIC33 analog input/output pins are routed to the J13 and J14 connectors on an AIC33 EVM board .

By stacking four AIC33 EVMs, all of the corresponding analog input/output pins of the four AIC33s are connected together.

2.3.1 Analog Inputs

There is no circuitry problem in connecting all of the corresponding inputs from the four AIC33 devices in the stacked EVM system. Keep in mind that an audio input signal sent to an AIC33 goes to the same pin(s) at the other three AIC33 codecs.

2.3.2 Analog Outputs

With four AIC33EVMs stacking together, the corresponding analog output pins of different AIC33 devices will be shorted, which could cause a problem if more than one output from different AIC33 codecs was powered up at the same time.

Thus, for this four-AIC33EVM and one-USB-MODEVM stacked system, it is **strictly forbidden** to enable the same audio output pins of different boards simultaneously.

Even though all differential output pins enter a 3-state mode at power down, the headphone output pins, HPLOUT, HPROUT, HPLCOM, and HPROUT, do not. The four pins have two programmable states when they are not powered up: weakly driven to VCM; or in a 3-state mode (default). Keep these pins in the 3-state mode during power down. That is:

- Set D2/Reg51/Page0 =1 for HPLOUT to a 3-state mode when powered down.
- Set D2/Reg58/Page0 =1 for HPLCOM to a 3-state mode when powered down.
- Set D2/Reg65/Page0 =1 for HPROUT to a 3-state mode when powered down.
- Set D2/Reg72/Page0 =1 for HPRCOM to a 3-state mode when powered down.

Note that this limitation is only for the AIC33EVM stacking system, but not for the general four-AIC33 system, as shown in Figure 1, because the audio outputs of the multiple codec system are not normally connected together .

3 Hardware and Connection

This section provides the step-by-step instructions for stacking four AIC33EVM boards on top of one USB-MODEVM board, so as to connect and test the multiple codec system.

Step 1: On the USB-MODEVM board, change JMP6 from *USB* (1~2) to *REG* (2~3).

Step 2: On the USB-MODEVM board, disable the I^2S connection from TAS1020B to the rest of the circuitry, by switching OFF SW2-4.

Step 3: On each of the AIC33EVM boards, ensure that the AIC33 device' SELECT pin is *low* (set JMP10 to 3~5 on the AIC33EVM boards). Set the address pins differently within the four EVMs.

Step 4: Stack an AIC33 EVM board (A1A0=00) on the top of the USB-MODEVM board, with J13, J14, J16, J17, and J15 on AIC33 EVM being plugged into J11, J21, J12, J22, and J23 on the top of the USB-MODEVM board, respectively.

Step 5: Power up the one AIC33EVM plus one USB-MODEVM system, through the J8 or J9 (from 6VDC to 10VDC), and check the power supplies (JMP4~JMP8), grounds, and signals on the first AIC33EVM board, to ensure that all are connected and working properly.

Step 6: Remove the power to the system, and continue to stack the rest of the AIC33EVM boards one on top of another. When done, repeat the Step 5 to check again.

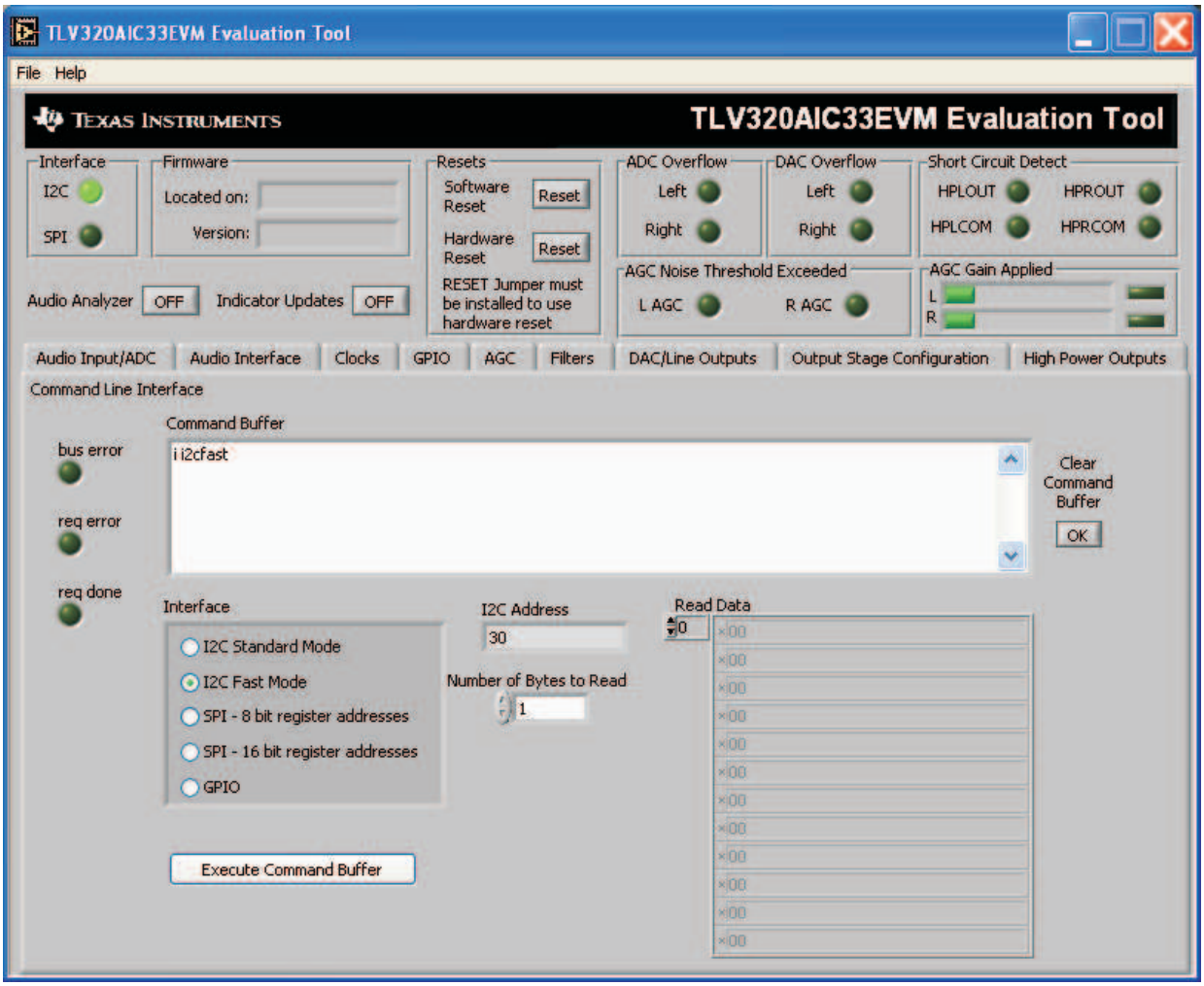
Step 7: Remove the power and conclude the hardware connection.

4 Software Script

To run the four-AIC33 codecs system, certain control registers inside each of the AIC33 should be set up by software. The appendix of this application report provides a script, 4Stacked_AIC33Test_EVM.txt, which was tested with the system discussed in section 3.

To run the script, follow these steps:

1. Start the AIC33EVM SW.
2. Select *I2C* when asked to *Select Control Interface Mode*.
3. Click on *OK* when asked *What are the settings for A0 and A1?*
4. Go to the *Command Line Interface* tab, and the following screen displays.



5. From the *File* menu on the upper-right corner of the screen, select *Open Command File* …, navigate to the location where the script was stored, and open the script to the Command Buffer in this tab.
6. Click on the *Execute Command Buffer* button to run the script.
7. Click on *OK* for all pauses during the running.
8. The *req done* LED on the left of the *Command Buffer* should become green to indicate the script has been finished successfully.

More details on AIC33EVM SW GUI can be found in the user's guide SBAU114.

5 TDM Test Results

Figure 3 to Figure 6 show the TDM bus timings under the four AIC33 devices' TDM mode. Where:

- Ch 1 is BCLK, which is 256×44100 = 11.2896 MHz.
- Ch 2 is the WCLK, which is 44.1 kHz.
- Ch 3 is connected to AIC33s' DIN, through which the host processor should send DAC data.
- Ch 4 is connected to AIC33's DOUT, through which the ADC data from each of the AIC33 devices are sent to the host.

Note that the MCLK to the system is 44100×256 = 11.2896 MHz; the first AIC33 (A1A0=00) is the TDM bus master, which generates the BCLK and WCLK; and the TDM word length has been set to 16 bits. (The AIC33 audio data word-length can be set to 16, 20, 24, or 32 bits).

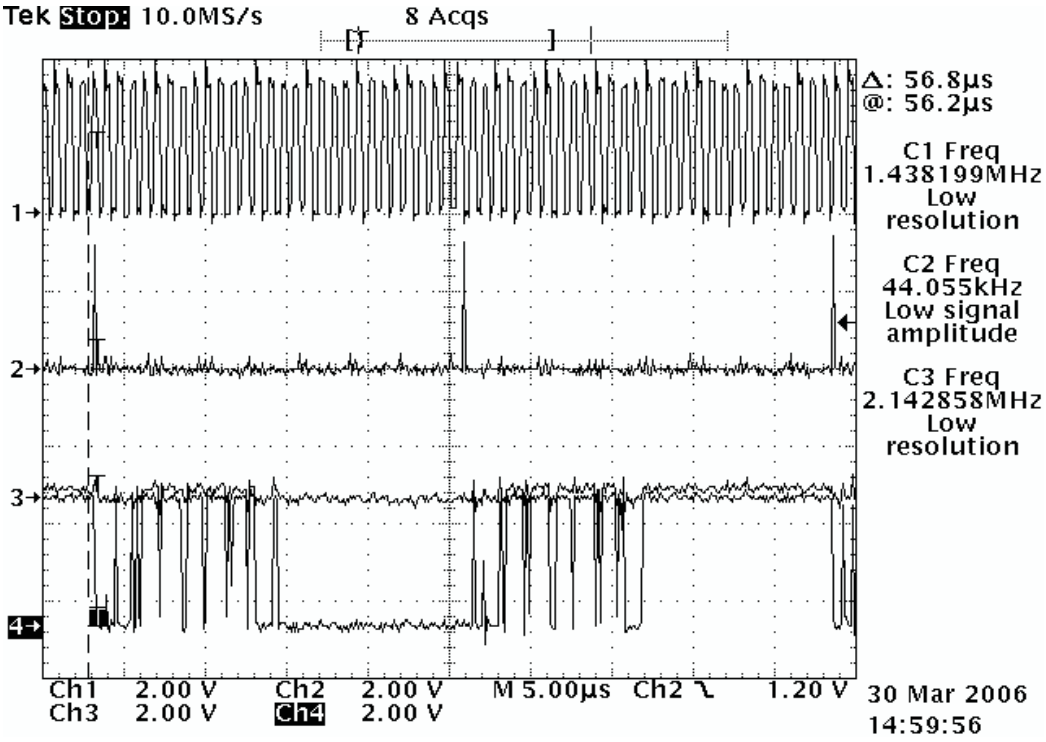


Figure 3. Four AIC33 Devices TDM Bus

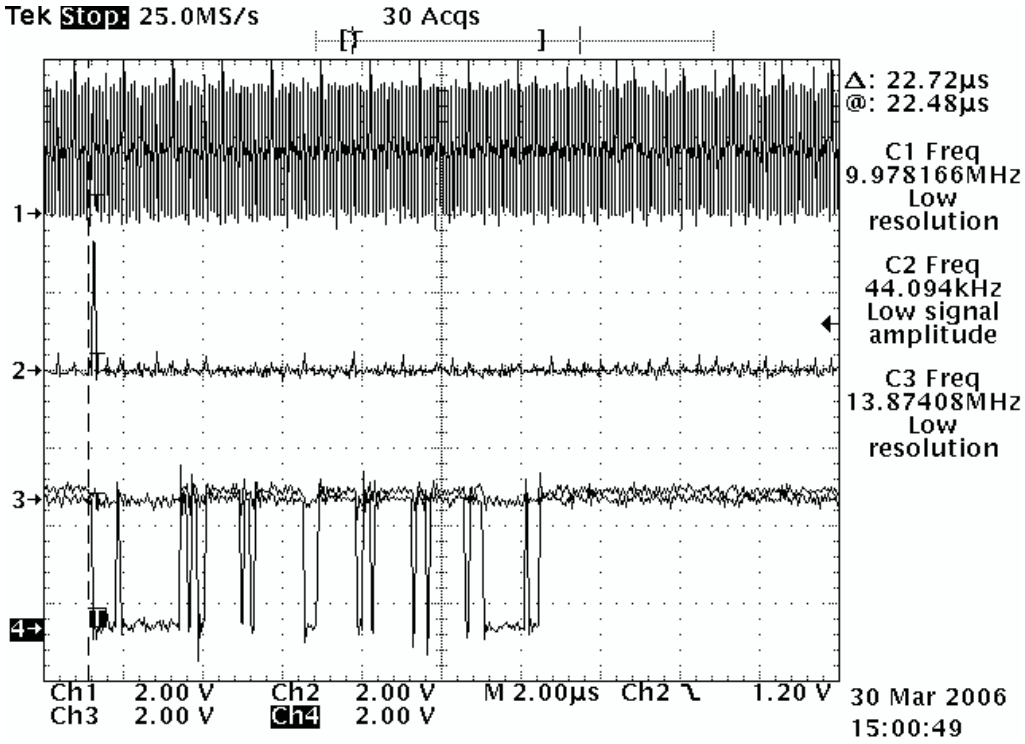


Figure 4. Four AIC33 Devices TDM Bus (Details Within a Frame)

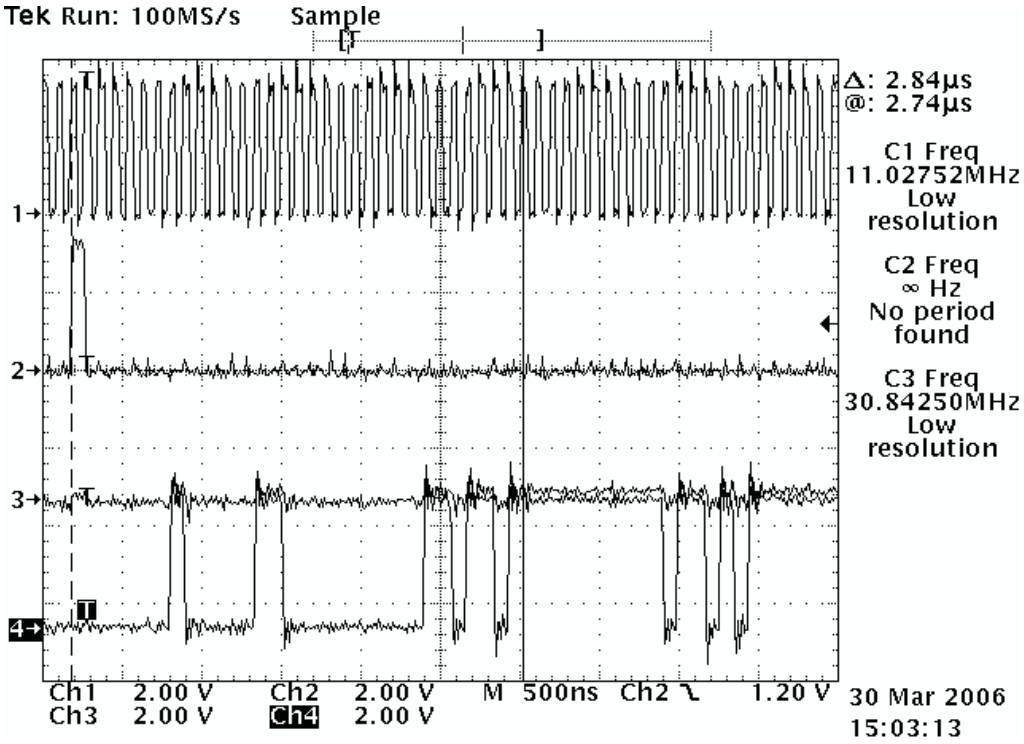


Figure 5. Four AIC33 Devices TDM Bus (Details Within the First AIC33)

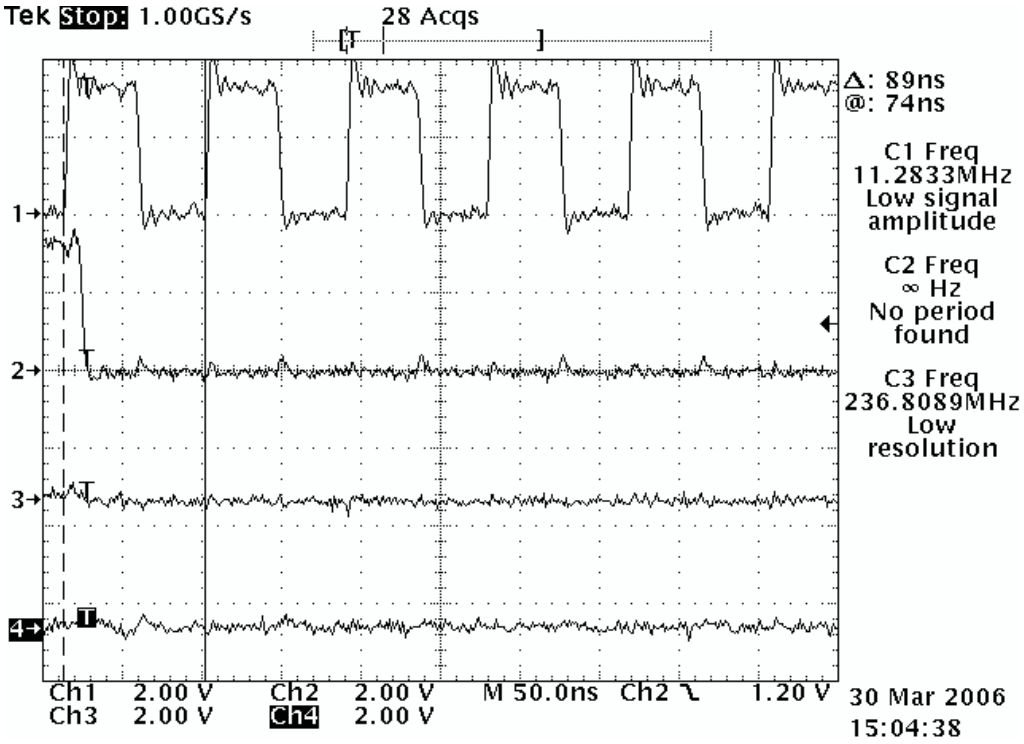


Figure 6. Four AIC33 Devices TDM Bus (Details on BCLK)

6 Conclusion

- The four AIC33 codec devices must work using the I^2C control bus mode, with different address (A1, A0) configurations, so as to share the same single control bus and to be controlled through a single host processor, such as the USB-MODEVM and its PC software.
- In order to share the same single audio data serial bus among the four AIC33 codecs, all codecs must work using the digital interface's TDM mode, with different offset bit settings. To build the system shown in Figure 1 using a USB-MODEVM and four-AIC33 EVM boards, you need to disable the connection for the audio data from the USB-MODEVM board, and to provide an external host processor with TDM interface to read/write the audio data from/to the four AIC33 devices.
- The TDM bus needs a *master* that generates the TDM clock and frame. The TDM bus master can be a host processor/DSP/CPU, or one of the four AIC33 codecs.

7 References

1. *TLV320AIC33, Low Power Stereo Audio CODEC for Portable Audio/Telephony* data sheet (SLAS480)
2. *TLV320AIC33EVM and TLV320AIC33EVM-PDK User's Guide* (SBAU114)
3. *Using TLV320AIC3x Digital Audio Data Serial Interface With Time-Division Multiplexing Support* application report (SLAA311)

Appendix A AIC33EVM Software Script

This appendix provides the AIC33EVM software script for setting up and running the four-AIC33 EVM stacked system as discussed in this application report.

```
#################################################################
# setup for 4 AIC33 EVM boards Stocked on a USB-MODEVM
#
# uses I2C interface and TDS audio data Interface
#
# Wendy Fang, 2006.3.29
#################################################################
#
# -- Digital Interfaces
#    The first EVM board (A1A0=00) is the TDM master to generate BCLK and WCLK
#
# -- Audio Inputs
#    For all 4 Boards, the audio input path are the same and:
#     MIC3 -> ADC PGA ----------------> ADC ->  DOUT
#    But ONLY one EVM ADCs is powered up and ONLY one MICBIAS should be enabled.
#
# -- Audio Outputs
#    Only one EVM outputs will be setup and enabled at a time and it is:
#     DIN --> Digital Volume Control -> DAC -> DAC_R1 -> Analog Volume Control -> HPOUT
#
#################################################################
#  -- input from MIC3
#  -- add power up MICBIAS to 2.5V
#
#  -- Output with pop reduction
#  -- Output at Capless mode from HPOUT
#################################################################
##############
# Interfaces
##############
# Since Fsref=44.1K (For: MCLK=11.2896MHz), we do not use PLL and FS=Fsref
#
# reg 07 - codec datapath
# L-DAC plays DIN left data and R-DAC plays right one
w 30 07 8A
w 32 07 8A
w 34 07 8A
w 36 07 8A
# reg 08/09/10 - Audio Interface
# The first codec is the master (-256s) and the rest are slaves;
# DOUT all at tri-state when valid data is bit being sent
# DSP/16-bit mode with slot (n*2*16 bits, n=0, 1, 2, 3) delay
w 30 08 E0
w 32 08 20
w 34 08 20
w 36 08 20
w 30 09 48
w 32 09 48
w 34 09 48
w 36 09 48
w 30 0A 00
w 32 0A 20
w 34 0A 40
w 36 0A 60
```

```
# Read back for debugging
r 30 07 4
b
r 36 07 4
b

###############
# Input Path
###############
# reg 17/18 - MIC3L for Left ADC and MIC3R for right ADC
w 30 11 0F F0

# regs 25 - Power up MICBIAS to 2.5V for only one of EVMs
w 30 19 00
w 32 19 00
w 34 19 00
w 36 19 80

# reg 19/22 - power up ADC
w 30 13 7C
w 32 13 7C
w 34 13 7C
w 36 13 7C

w 30 16 7C
w 32 16 7C
w 34 16 7C
w 36 16 7C

# regs 15/16 - unmute ADC PGA and set to 0dB
w 30 0F 00 00
w 32 0F 00 00
w 34 0F 00 00
w 36 0F 00 00

# Read back
r 30 0F 0B
b
r 36 0F 0B
b

###############
# Output Path
###############
# reg 14 - if at AC-Cap mode
#w 36 0E 80

# reg 42 - driver power ON Pop Control
w 30 2A 6C
w 32 2A 6C
w 34 2A 6C
w 36 2A 6C

######
# reg 37 DAC POWER CONTROL/ reg 38 HPCOM CONFIG
# Power up L and R DACs
# HPCOML/R as Headphone COM for Cap-Less mode
w 36 25 D0 08

# regs 43/44 - Unmute DAC L/R and set the Digital Volumes to 0dB
w 36 2B 00 00

# Read back
r 30 25 8
b
r 36 25 8
b

######
# reg 47 - HPLOUT from Left DAC routed to HPLOUT @ 0dB
w 36 2F 80

# reg 51 - HPLOUT Level = 0dB, not muted, and powered up
w 30 33 04
```

```
w 32 33 04
w 34 33 04
w 36 33 0D

# reg 58 - HPLCOM Level, set HPLCOM at tri-state with PD
w 30 3A 04
w 32 3A 04
w 34 3A 04
w 36 3A 04

#Read Back
r 30 2F 12
b
r 36 2F 12
b

# reg 64 - HPROUT from Right DAC routed to HPROUT @ 0dB
# reg 65 - HPROUT Level = 0dB, not muted, and powered up
w 30 40 80 04
w 32 40 80 04
w 34 40 80 04
w 36 40 80 0D

# reg 72 - HPRCOM Level, set HPRCOM at tri-state with PD
w 30 48 04
w 32 48 04
w 34 48 04
w 36 48 04

# Read back
r 30 40 9
b
r 36 40 9
```

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265