Interfacing With the DAC8541 Digital-to-Analog Converter

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ABSTRACT

This application report shows how to interface and operate the DAC8541 with a commercially available microprocessor or Texas Instruments DSP. Although this report uses a TMS320C31™ DSP as an example for the host interface, the concept is generic in nature and therefore should fit any host processor selected to interface with this DAC. This report bridges the gap between digital signal system processing and analog signal processing.

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TMS320C31 DSP is a trademark of Texas Instruments.

1 Introduction

Interfacing between the digital domain and the analog domain seems to be a common problem for some engineers. This is true especially when the user is not particularly familiar with the device's pin terminology or functionality. This application report talks about the pin terminologies for the DAC8541 and explains their functions. Any unclear or missed definitions in the data sheet are covered here. It also talks about other areas of concern and presents a solution for getting this DAC in proper working condition.

The DAC8541 EVM is discussed here as an evaluation platform that is used to demonstrate the complete circuit implementation for the functional test of this DAC.

2 DAC8541 Overview

The DAC8541 is a high resolution, low power DAC with a built-in precision amplifier that allows rail-to-rail voltage output swing. This DAC supports the parallel interface using a 16-bit word data format common to most microprocessors or DSPs. The DAC8541 offers 16-bit monotonic performance with a typical ±0.003% FSR settling in 10 μs. There are some added features that are built into this DAC which makes it an indispensable part of any data acquisition system. These features are: the power-down function to reduce power consumption, power-on-reset to ensure the DAC's output is at a known state during power-up, asynchronous output update (LDAC), and reset capability that is hardware enabled. The DAC8541 also features a split-core supply for better control of noise. An external reference voltage is required to set the output range of the DAC.

The DAC8541 is recommended for process control, data acquisition, closed-loop servo control, and many more applications in the industrial process market. It is also equally applicable for high-resolution applications in the test and measurement market and portable instrumentation.

3 DAC8541 EVM

The DAC8541 evaluation module is designed as a quick and easy way to evaluate the high resolution, single-channel, parallel input DAC. The evaluation module features a parallel interface to communicate to any host processor base system.

Some initial configuration is required to operate the EVM. Also, a customize cable to adapt the EVM to the host platform is required if a TI DSK is not used. A dc output power supply is needed to provide power to the EVM. The ±15 V supply provides power to the built-in reference circuit and the output stage amplifier. The built-in reference is included in the EVM board, since an external reference is required to set the output range of the DAC8541. The external reference onboard the EVM can be disconnected if the users desire to apply their own reference voltage. The variable 5 V supply provides power for the DAC's AV_{DD} and DV_{DD} input. The analog and digital supplies should be connected at the power supply, which means that separate pairs of wires are needed for AV_{DD} and DV_{DD} input. If a single pair of wires is used, then AV_{DD} and DV_{DD} should be tied together at the power supply input terminal, and jumper W8 must be closed.

The data and control pins are accessible through the connectors J1, J2, and J3. Figure 1 displays the mapping of the pins to their respective connectors. All the even numbered pins of J1 are tied to DGND while J2 and J3's unconnected pins are left floating (see the schematic in Figure A–1).

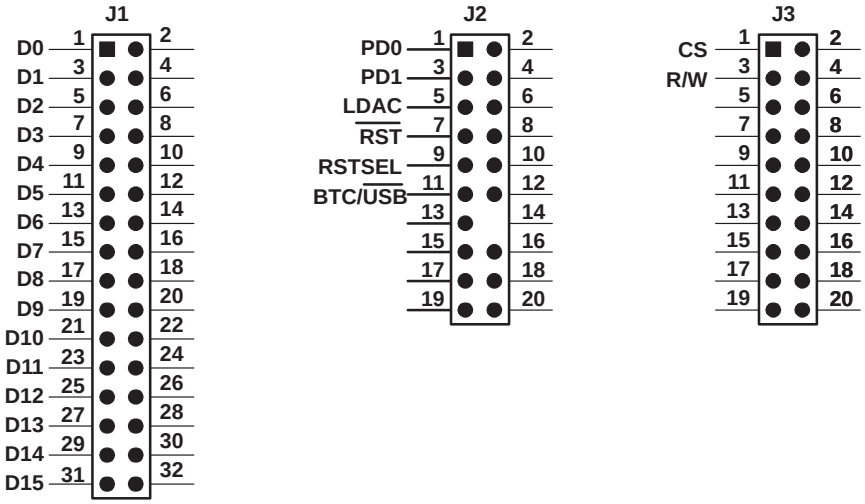


Figure 1. I/O Mapping of the DAC8541 EVM

The DAC8541 EVM is fabricated on a two-layer printed-circuit board using a copper-clad FR4 laminate material. The PC board layout is designed with the minimum trace length possible to minimize the effects of parasitic capacitance and inductance. For this reason, surface-mount components are used to achieve the highest level of performance of the DAC8541.

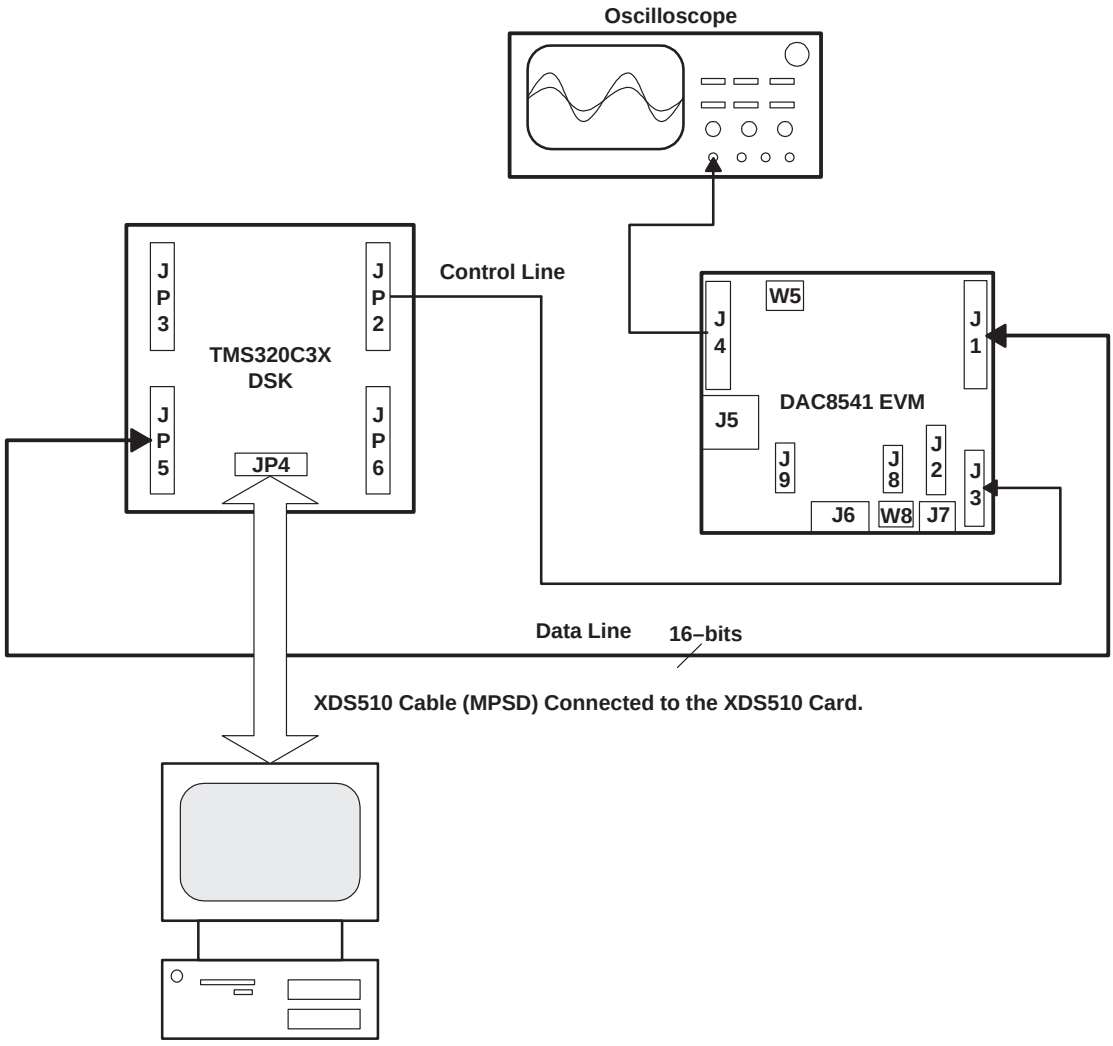
A separate grounding scheme for digital and analog is implemented, and the analog and digital signals are also isolated from each other, where possible, to minimize the noise. This approach may not necessarily yield the best performance result with certain individual designs. In any case, thoroughly bypassing the power supply and reference pins of the DAC8541 is strongly recommended.

Table 1 shows the default jumper settings for the DAC8541 EVM board.

Table 1. Default Jumper Settings

REFERENCE	JUMPER POSITION	FUNCTION
W1	1–2	$V_{REF}L$ is tied to AGND
W2	1–2	The onboard REF02 is used for external reference
W3	1–2	Negative supply rail of output Op-amp requires –15-V supply
W4	1–2	Positive supply rail of output Op-amp requires 15-V supply
W5	3–4	DAC output signal is buffered
W6	CLOSED	External op-amp is bipolar output configuration
W7	CLOSED	External op-amp is bipolar output configuration
W8	CLOSED	AGND and DGND are tied together

A block diagram of the hardware interface connection of the DAC8541 EVM to the TMS320C31 DSK including other peripherals needed for this application is shown in Figure 2.



Note: The XDS510 Card is installed inside the PC.

Figure 2. Hardware Block Diagram

4 Pin Descriptions and Functionality

4.1 Reset Function

The DAC8541 has a built-in power-on-reset (POR) circuit that puts the device into a known state upon power up. The DAC powers up at minimum scale and stays there until a valid write takes place to the device. This is a useful feature for applications that require the DAC output be in a known state while the system is powering up.

In addition, a hardware-enabled reset ($\overline{\text{RST}}$) is also featured in this device to enable resetting the DAC output to either min-scale or mid-scale, depending on the state of the reset select (RSTSEL) input pin. If RSTSEL = 0, then DAC output is min-scale, otherwise if RSTSEL = 1, then the DAC output is mid-scale. The reset function does not change or affect the input data register. Refer to Figure 2 of the data sheet (SLAS353) for the correct reset timing.

4.2 Power-Down Function

The power-down function features four modes of operation and is programmable through two input pins, PD0 and PD1, to the device. Refer to Table 3 of the data sheet for the different modes of operation. When the PD0 and PD1 pins are both set to zero, the DAC operates in normal mode with its typical power consumption of 250 μA at AV_{DD} = 5 V (50 nA at AV_{DD} = 3 V). Normal mode is also the default mode of the DAC. When the DAC is programmed in the power-down state, the supply current is reduced and the V_{OUT} terminal is internally switched from the output of the amplifier to a resistor network. The output impedance of the DAC depends on the state of PD0 and PD1 in power-down mode. Refer to Table 3 of the data sheet.

In addition, the analog circuitry of the DAC is shut down when in power-down mode but the contents of the DAC registers are unaffected. This allows the DAC's output voltage to return to the previous level when it is powered up again. It takes typically 2.5 μs for AV_{DD} = 5 V or 5 μs for AV_{DD} = 3 V for the DAC to come out of power-down mode and resume the normal mode of operation.

4.3 Data Format

The DAC8541 features two data I/O formats, which are made available to the host processor interface. These two formats are the binary 2s complement (BTC) and the unipolar straight binary (USB). The BTC/$\overline{\text{USB}}$ input pin controls the format used by the DAC. The selected data format is used for data written into the device as well as data that is read back from it. Refer to Table 2 of the data sheet for the data format.

4.4 LDAC Function

The DAC8541 is designed using a double-buffered architecture by implementing an input register and an output register. A write command transfers data to the input register through the data input pins. The data is held in the input register until a rising edge of load DAC (LDAC) is detected. The rising edge of LDAC transfers the data from the DAC input register to the DAC output register. As soon as the rising edge of LDAC is issued, the DAC output begins to settle with the new value written to the DAC output register. The data in the DAC input register does not change when the LDAC command is given. The minimum LDAC signal pulse required is 40 ns each for both HIGH and LOW duration.

4.5 Voltage Reference Inputs

$V_{REF}H$ and $V_{REF}L$ input pins are provided to set the voltage output range of the DAC. A typical rail-to-rail operation requires that the $V_{REF}H$ input be equivalent to AV_{DD} and that $V_{REF}L$ input be tied to AGND. The $V_{REF}L$ input can accept a small amount of voltage ranging from –100 mV to 100 mV for minor output offset adjustments with respect to AGND. Because of the reference architecture of the DAC, the voltage output is affected by the difference between $V_{REF}H$ and twice the $V_{REF}L$ input.

The equation for V_{OUT} is then given below as:

$$V_{OUT} = [V_{REF}H – (2 \times V_{REF}L)] \times [D \div 65536]$$

Assuming there is no offset or gain error, then $V_{REF}L$ = AGND, therefore, the ideal voltage output equation is given by:

$$V_{OUT} = [V_{REF}H] \times [D \div 65536]$$

If an adjustment is necessary, the output impedance of the source for reference voltage must be very low, so the accuracy of the DAC over its operating range is not affected.

4.6 Analog and Digital Supplies

The architecture of the DAC8541 is designed to accept two separate power supplies to operate and achieve optimum performance, eliminating as much noise as possible that can affect the output. The analog supply, AV_{DD}, powers the analog section of the DAC architecture, such as the output amplifier and the main DAC core. The digital supply, DV_{DD}, powers the digital architecture of the DAC. The digital supply sets the voltage threshold of the control and data I/O of the DAC. The voltage range of the AV_{DD} input is a minimum of 2.7 V up to a maximum of 5.5 V, while the DV_{DD} input can independently function from a range of 1.8 V minimum up to a maximum of 5.5 V.

The grounding approach implemented on the DAC is also separate between AGND and DGND. With this technique a true dual-supply operation is achieve to optimize the DAC performance by having better control of the return currents from both analog and digital side.

5 Host Processor Operation

The host processor drives the DAC, so the proper operation of the DAC depends on the successful configuration between the host processor and the EVM board and a properly written code to run the DAC.

A custom cable made specific to the host interface platform is required to allow exchange of data between the host processor and the DAC. The EVM allows interface to the host processor through J2 and J3 header connectors for control signals, and J1 header connector for the data input, as shown in Figure 1 of this report. The output can be monitored through the J5 BNC connector (if installed) or J4 header connector. An interface adapter card is also available for specific DSP starter kits. Refer to the DAC8541 EVM user's guide manual for more information on obtaining an interface adapter card.

A detailed description of the hardware interface is shown in Figure 3, interfacing the DAC8541 to the TMS320C31 DSP. The other control pins are tied statically to DGND or DV_{DD} as described in Table 2, but they can be actively controlled if necessary using available GPIO pins or any usable pins of the DSP.

The hardware configuration is quite discreet, and it becomes more so, if only one DAC is interfaced with the host processor, as it is in this application example. An address decoder can be implemented when multiple devices are used to properly select the device to be addressed. The address decoder must be enabled by the $\overline{\text{STRB}}$ signal to conform to the proper $\overline{\text{CS}}$ timing requirements specified in the data sheet.

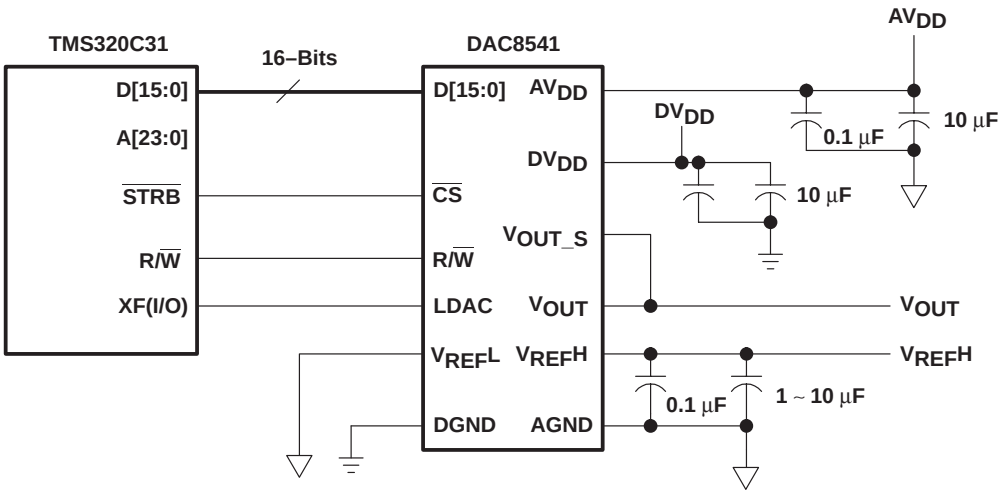


Figure 3. DAC8541 to TMS320C31™ DSP Hardware Interconnect

Table 2. Control Pin Settings

PD0	Tied to DGND
PD1	Tied to DGND
$\overline{RST}$	Tied to DV_{DD} via pullup resistor
RSTSEL	Tied to DGND
BTC/$\overline{USB}$	Tied to DGND

Once the DSP is configured for this specific operation (refer to SLAU071 for DSP parallel configuration) the DAC8541 operation becomes very simple since it only requires a few stimuli to get going. It is much more simple if the DAC8541 is the only device that the host processor is interfacing with, since $\overline{CS}$ and R/$\overline{W}$ pins can also be statically tied to DGND. Tying R/$\overline{W}$ pin statically to DGND is only recommended if a read function is not intended to be performed on the device. This is another way to simplify the circuit design further. Although the host processor no longer drives the $\overline{CS}$ and R/$\overline{W}$ pins of the DAC, it does not mean that these signals can now be ignored in the host processor side. The correct read/write timing for the host processor must still be observed according to the host processor's data sheet specification. Regardless of the interface configuration, the LDAC input pin must be controlled since this is the only way that the DAC output gets updated. If the $\overline{CS}$ and R/$\overline{W}$ pins are tied to DGND, the LDAC signal must be asserted no earlier than 10 ns from when the input data becomes valid.

Referring back to the interface connection in Figure 3, the 16-bit parallel data becomes valid when a valid R/$\overline{W}$ and $\overline{CS}$ occurs. Once the data is transmitted into the DAC input register, the LDAC signal must be toggled to update the output of the DAC as described earlier in the LDAC section.

A program that shows the DAC8541 operation is included in Appendix A of this report. The program stimulates the digital input pattern, and the DAC processes these stimuli and displays the series of sinusoidal waveform pattern that are observed by probing on the DAC output pin.

6 Summary

This application report describes how simple the DAC8541 is operated and how it interfaces with any microprocessors or TI DSP available in today's market. With the ease of use of this product, as presented in this report, it allows design engineers to speed up their design implementation and meet their time to market requirements. This is always a positive factor when it comes to delivery and execution of products.

This application report also goes into detail in describing the functions of the important control pins of this DAC and it covers most of the features. One thing to keep in mind is the voltage range of the digital thresholds, which goes as low as 1.8 V, allowing any host processors operating at this threshold voltage to be still compatible with this DAC.

7 References

1. *DAC8541 data sheet* (literature number SLAS353)
2. *DAC8541 EVM User's Guide* (literature number SLAU085)
3. *TMS320C3x User's Guide* (literature number SPRU031)
4. *Interfacing the TLV5639 DAC to the TMS320C31 DSP* (literature number SLAU071)

Appendix A DAC8541.ASM

The program to run a sinusoidal waveform is shown below and includes the command and vector files.

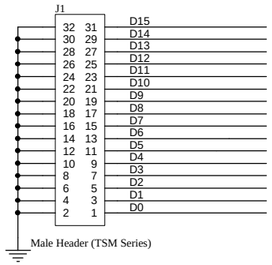
```
************************************************************************
* DAC8541.asm
* Author: Joselito Parguian
* Company: Texas Instruments
************************************************************************
            .title    "DAC8541.ASM"
            .global   START
            .data
DAC1        .set      1          ; DAC8541 DAC Access
DAC_BASE    .word     80A000h    ; use this external addresses 80A000h or
                                 ; 0C00000h as base address for DAC
p_buscon    .set      808064h    ; Primary bus control
timer1      .set      808030h    ; Timer1 Global Control
t1_ctr      .set      808034h    ; Timer1 Counter
t1_prd      .set      808038h    ; Timer1 Period
            .data
table .int   32768,33572,34376,35178,35980,36779,37576,38370,39161,39947,40730,41507,42280
   .int  43046,43807,44561,45307,46047,46778,47500,48214,48919,49614,50298,50972,51636
   .int  52287,52927,53555,54171,54773,55362,55938,56499,57047,57579,58097,58600,59087
   .int  59558,60013,60451,60873,61278,61666,62036,62389,62724,63041,63339,63620,63881
   .int  64124,64348,64553,64739,64905,65053,65180,65289,65377,65446,65496,65525,65535
   .int  65525,65496,65446,65377,65289,65180,65053,64905,64739,64553,64348,64124,63881
   .int  63620,63339,63041,62724,62389,62036,61666,61278,60873,60451,60013,59558,59087
   .int  58600,58097,57579,57047,56499,55938,55362,54773,54171,53555,52927,52287,51636
   .int  50972,50298,49614,48919,48214,47500,46778,46047,45307,44561,43807,43046,42280
   .int  41507,40730,39947,39161,38370,37576,36779,35980,35178,34376,33572,32768,31964
   .int  31160,30358,29556,28757,27960,27166,26375,25589,24806,24029,23256,22490,21729
   .int  20975,20229,19489,18758,18036,17322,16617,15922,15238,14564,13900,13249,12609
   .int  11981,11365,10763,10174,9598,9037,8489,7957,7439,6936,6449,5978,5523,5085,4663
   .int  4258,3870,3500,3147,2812,2495,2197,1916,1655,1412,1188,983,797,631,483,356,247
   .int  159,90,40,11,1,11,40,90,159,247,356,483,631,797,983,1188,1412,1655,1916,2197
   .int  2495,2812,3147,3500,3870,4258,4663,5085,5523,5978,6449,6936,7439,7957,8489,9037
   .int  9598,10174,10763,11365,11981,12609,13249,13900,14564,15238,15922,16617,17322
   .int  18036,18758,19489,20229,20975,21729,22490,23256,24029,24806,25589,26375,27166
   .int  27960,28757,29556,30358,31160,31964
t_addr.int  table
;-------------------------------------------------------
      .text
START ldp   @p_buscon              ;
      ldi   01018h,R0              ; (01018h=256 BC,0WS)
      Sti   R0,@p_buscon           ; 0-ws, /RDY pin logically AND'ed
      ldi   066h,IOF               ; XF0 = 1 (output disabled) LDAC
      ldi   @DAC_BASE,AR0          ; set address of DAC
      ;----------------------
      ldi   0FFFFh,R2              ; word mask
```

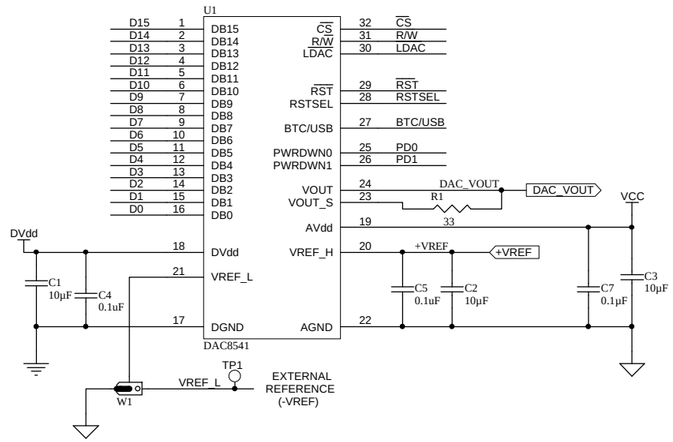
```
      ldp   t_addr
LOOP  ldi   @t_addr,AR1              ; load start of table address
      ldi   255,R1                   ; load table length
AGAIN
      ldi   *AR1++,R0                ; Generate sinewave
      and   R2,R0                    ; mask data
      sti   R0,*+AR0(DAC1)           ; Send data out to DAC
      ldi   022h,IOF                 ;
      ldi   066h,IOF                 ; Update DAC output
      subi  1,R1
      bnz   AGAIN
      b      LOOP
;-------------------------------------------------------
   .end
/*************************************************************/
/* Generic C31 linker command file for the using only        */
/*    2k internal memory                                     */
/*************************************************************/
MEMORY
{
      RAM0: org = 0x809800 len = 0x400      /* RAM BLOCK 0  0x0fe */
      RAM1: org = 0x809C00 len = 0x3C1      /* RAM BLOCK 1  0x1ff */
      VECS: org = 0x809fc4 len = 0x010      /* INTERRUPT VECTORS  */
}
SECTIONS
{
      .text:       > RAM0                   /* CODE               */
      .data:       > RAM1                   /* DATA               */
      "int3_isr"   > RAM0                   /* ISR                */
      "vectors"    > VECS                   /* Interrupt Vectors  */
}
*******************************************************************************
* VECTORS.ASM
* This is where all interrupt vectors are defined. The user can add here any specific
* interrupt vectors that will be used in the program
*******************************************************************************
      .title"VECTORS.ASM"
      .ref  START
      .sect ".vectors"
RESET:.int  START          ; External reset
```

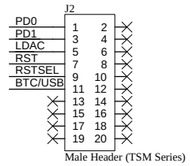
Figure A–1. Schematic Diagram of the DAC8541 EVM

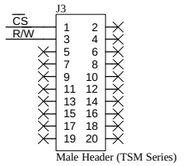
The schematic diagram of the DAC8541 EVM is located on the following page.

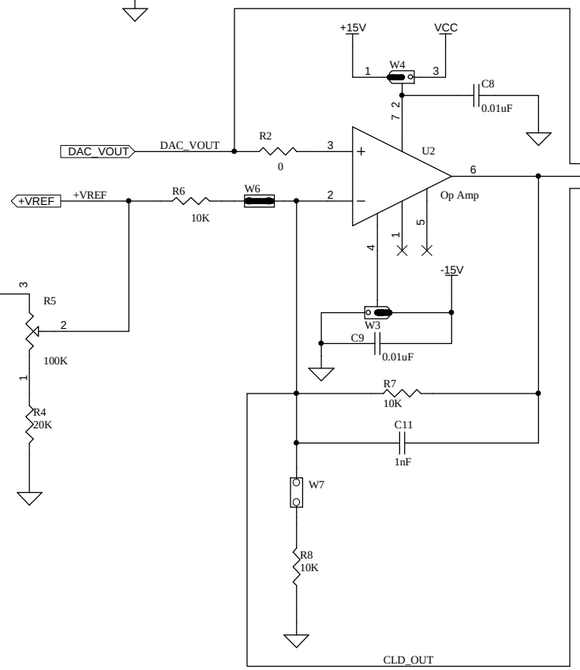
Revision History		
REV	ECN Number	Approved

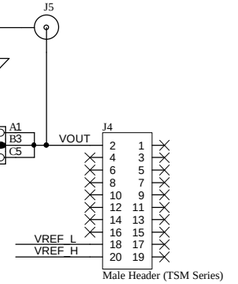


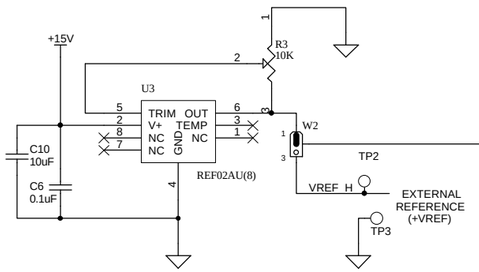


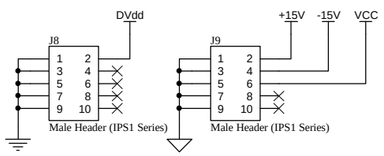


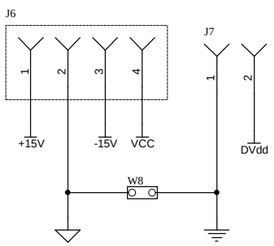












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	12500 TI Boulevard. Dallas, Texas 75243
Title:	DAC8541
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6435625 — REV: A
Drawn By:	
FILE: DAC8541.Sch	DATE: 3-May-2002 — SIZE: — SHEET: 1 OF:

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