Using References to Generate Offsets for the TLC55XX Family Data Converter

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ABSTRACT

This application report describes the process for using references to generate offsets for Texas Instrument's TLC55XX family data converters.

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Description

One common problem when interfacing to modern single supply A/D converters is biasing the analog input so that it is centered within the reference voltage range of the A/D. For the more common SAR type data converters it is often sufficient to set Vref top to V_{CC} and Vref bottom to GND. Then, biasing the midscale voltage of the input stage is simply a matter of generating $1/2V_{CC}$. This can be accomplished with a resistor divider network or, if more line/load stability is needed, by using the TLE2425 virtual ground or the TLE2426 rail splitter.

High-Speed Converters

Some high-speed converters such as the TLC5510, TLC5540, and TLV5580 have internal resistors that can be used to set internal reference voltages. On these devices, reference top (REFT) and reference bottom (REFB) pins are available. Normally, these pins would be used as reference inputs when an external reference is used. In this case we are relying on V_{DDA} and the internal divider to generate the reference voltages and take advantage of their availability. In Figure 1, the two 100 KΩ (R1, R2) resistors from REFT to REFB divide this voltage in half, generating a midpoint value between the top and bottom references. The small loading effect of these resistors only slightly moves the references and these can be taken into account in the DSP or other processor. The values shown for the internal reference divider resistors are the nominal values from the data sheet. Keep in mind that only the ratio of these internal resistors is accurate. The actual value of these internal resistors can vary by as much as 20%.

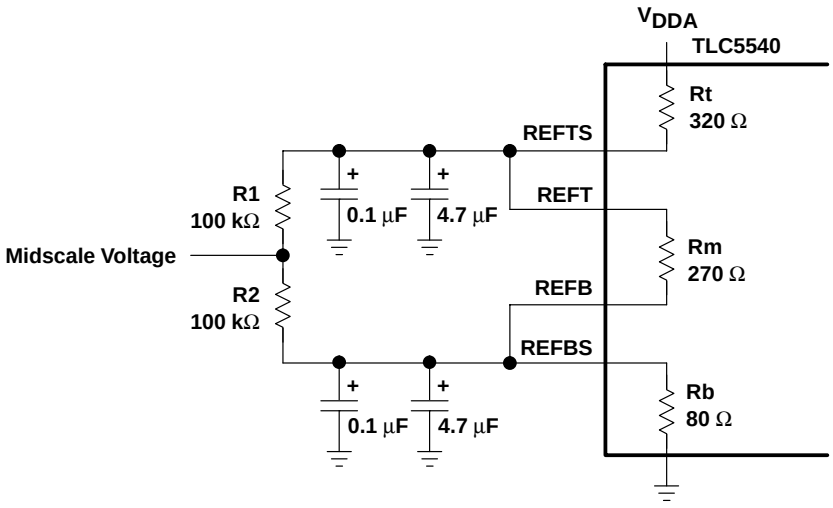

Figure 1. High-Speed Converter Basic Circuit

Figure 1 shows the high-speed converter basic circuit. One definite advantage to this technique is that the midpoint value will track ratiometrically to any variations in V_{DDA}.

$$\text{Midscale Voltage } (V_{ref}) = V_{Bot} + (V_{Top} - V_{Bot}) \times \frac{R2}{R_1 + R_2} \tag{1}$$

Where

$$V_{Top} = V_{DDA} \times \frac{\left(\frac{RM \times (R1 + R2)}{RM + R1 + R2}\right) + R_B}{R_T + \left(\frac{RM \times (R1 + R2)}{RM + R1 + R2}\right) + R_B} \tag{2}$$

and

$$V_{Bot} = V_{DDA} \times \frac{R_B}{R_T + \left(\frac{RM \times (R1 + R2)}{RM + R1 + R2}\right) + R_B} \tag{3}$$

Biasing Techniques for a Split Supply

Armed with this midpoint value, the following biasing techniques can be used with bipolar, dc coupled or ac coupled inputs to prepare them for processing by a single supply converter. The first technique, shown in Figure 2, gives a noninverting gain set by the two resistors R1 and R2.

$$V_o = V_{in}\left(1 + \frac{R1}{R2}\right) + V_{Midscale}\left(\frac{R1}{R2}\right) \tag{4}$$

The midscale voltage is inverted by the op-amp marked TLE2227(B) and a negative version of it is used for the offset. One requirement with this technique is that the amplifiers have a split supply for a bipolar input.

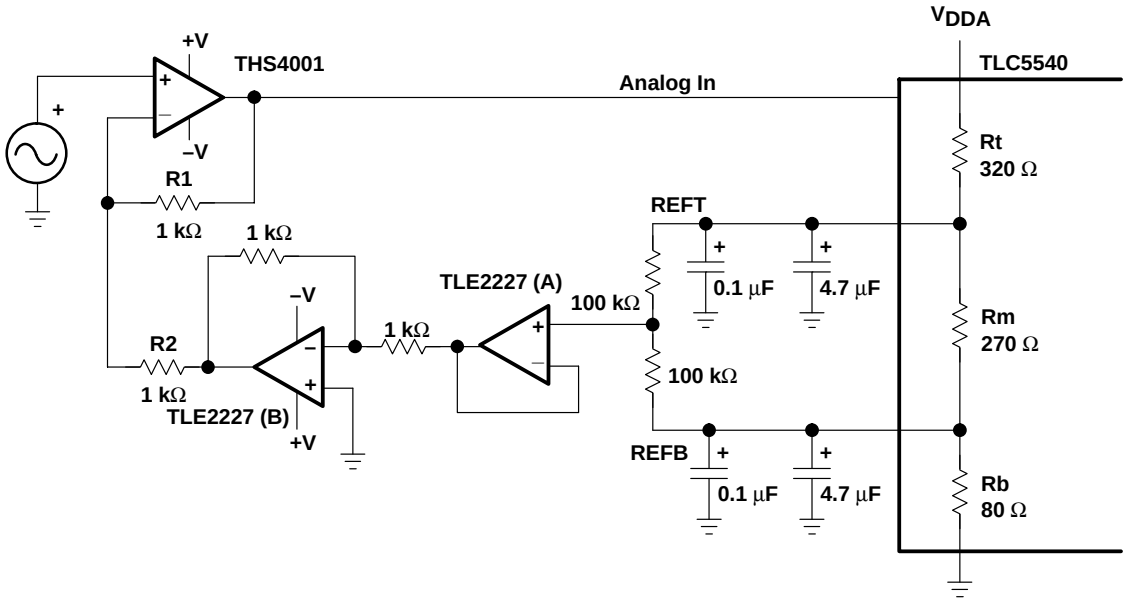

Figure 2. Example With Split Supply

Biasing Techniques for a Single Supply

If it is desired that the entire system operate on a single supply yet still be able to measure bipolar inputs, a slightly different technique is required. Figure 3 shows an example of this technique.

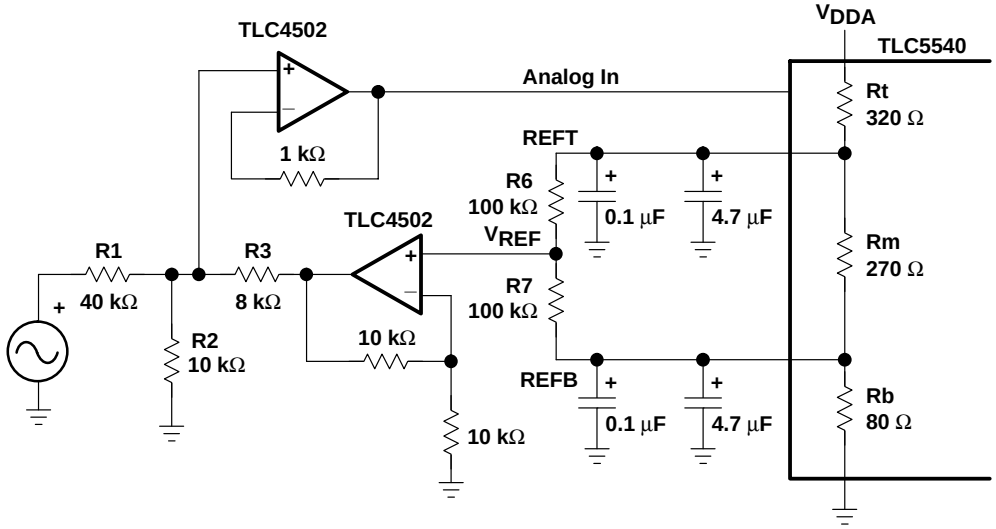

Figure 3. Example With Single Supply

To simplify the analysis of this circuit you can use the principle of superposition. In this case, consider that the incoming bipolar signal is larger than the span of the reference and therefore it needs to be attenuated. Also consider that the signal is centered at zero volts (other possibilities can be easily accounted for by adjusting the dividers). The resistance divider circuit made up of R1 and R2||R3 does the attenuating while the output of op-amp TLC4502 provides the offset needed through the divider network R3 and R1||R2.

As a real world example, consider that the input signal is a ±10 V signal that needs to be measured. First figure the full-scale span of the data converter which is the voltage at REFT minus the voltage at REFB. Doing math for a 5 V V_{DDA} , the span comes to about 2.01 V with a midpoint half way between 2.61 V and 0.597 V or about 1.6 V.

Now consider 2 V as the span, a 10:1 reduction is needed on the input signal, which means that R1 needs to be nine times the value of R2||R3.

In order to supply the midpoint voltage through a buffered source, a gain of 2 is introduced. The gain of 2 is then removed by the resistor divider network R3 and R1||R2.

The values arrived at are shown in Figure 3.

$$V_{out}(\text{Analog in}) = V_{in} \times \frac{R2||R3}{R1 + R2||R3} + 2 \times V_{ref} \times \frac{R1||R2}{R3 + R1||R2} \quad (5)$$

Where

$$R2||R3 = \frac{R2 \times R3}{R2 + R3} \text{ And } R1||R2 = \frac{R1 \times R2}{R1 + R2} \quad (6)$$

180 Degree Phase Shift

The circuit in Figure 4, introduces a 180 degree phase shift on the signal, but since far fewer resistors are required, it is much easier to meet the accuracy needs of the system. Note that resistors R6 and R7 are now different values. This is because of the amplifying effect of the inverting stage due to dc-coupling. If the calculations are done with these values, it is seen that a zero volt input is centered within the A/Ds reference range. If the input is ac-coupled, R6 and R7 must be the same value (i.e., 100 kΩ).

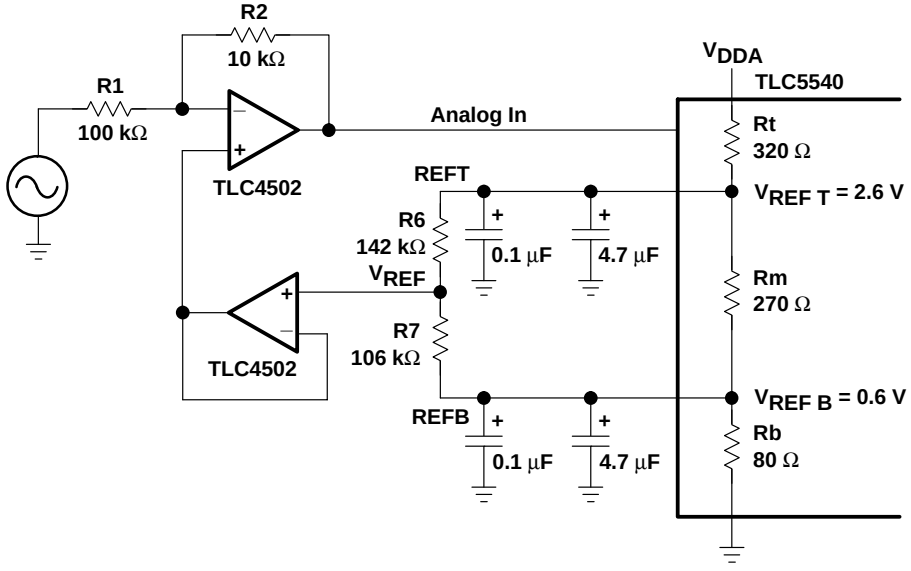

Figure 4. Circuit With a 180 Degree Phase Shift

$$V_{out} = V_{in}\left(-\frac{R2}{R1}\right) + V_{ref}\left(1 + \frac{R2}{R1}\right) \quad (7)$$

Where

$$V_{ref} = V_{Bot} + \left(V_{Top} - V_{Bot}\right) \times \frac{R7}{R6 + R7} \quad (8)$$

And, V_{Top}, V_{Bot} are derived as they were for Figure 1.

Power Supply and Layout Consideration

Power supply noise and circuit board layout are key to achieving desired performance for most high speed converters. Refer to application section of the data sheet of the converters you are using for power supply decoupling and layout recommendations. The evaluation module (EVM) for the TLC5510/5540 is also an example of proper layout and decoupling.

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