Fact Sheet

Military Semiconductor Products

SMJ320C6701/ 5962-9866101QXA

SGYV046M April 2002

840 MFLOPS (Million Floating Point Operations Per Second – peak) – 1 GFLOPS (Billion Floating Point Operations Per Second – peak) Floating point Digital Signal Processor (DSP)

HIGHLIGHTS

- The SMJ320C6701 is the highest performance military programmable floating point DSP available to the market. The C6701's performance capability is 840 MFLOPS and 1120 MIPS (Million Fixed-Point Instructions Per Second – RISC-like) at 140 MHz operation over the extended temperature range of -55°C to +115°C (W temp). Breakthrough performance isn't the only advantage of the C6701. Also available is the SM320C6701GLPS16 which provides 1 GFLOPS performance at 167 MHz over the extended temperature range (-40°C to +90°C). Using TI's revolutionary VelociTI™ architecture, the C6701 offers code compatibility and pin-for-pin compatibility with the 1200 MIPS 'C6201 fixed-point DSP. This means a single set of development tools and board-level device interchangeability that provides significant development, resource and manufacturing cost savings. Both the C6201B and C6701 devices are available in a 27x27 mm Ceramic Dimpled Ball Grid Array.

- Ada 95 compiler (http://www.ti.com/sc/docs/products/military/liter/adapress.pdf) (production versions available now)

- Advanced VLIW CPU Core operating at 1.9 V with 3.3-V on-chip peripherals and all I/Os

- TI added floating point capability to 6 of the 8 highly independent functional units (two of each type) found in the core of the fixed-point member of the C6000™ family…the C6201. Following is a list of the 4 different functional units found in the core of the C6701 and their fixed and floating point capabilities:

  - ✓ **L Unit:** 32/40-bit fixed point arithmetic and compare operations
    32/64-bit floating point arithmetic and compare operations (IEEE single and double precision)
    32-bit fixed point logical operations
    fixed/floating point conversions
    64 to 32-bit floating point conversions

  - ✓ **S Unit:** 32-bit fixed point arithmetic operations
    32/40-bit shifts and 32-bit bit-field operations branching and constant generation
    32/64-bit floating point reciprocal, absolute value, compares, and 1/sqrt operations
    32 to 64-bit floating point conversions

  - ✓ **M Unit:** 16 x 16-bit fixed point multiplies
    32 x 32-bit fixed point multiplies
    32 x 32-bit single precision floating point multiplies
    64 x 64-bit double precision floating point multiplies

  - ✓ **D Unit:** 32-bit add, subtract, linear, and circular address calculation
    8/16/32/64-bit loads
    8/16/32-bit stores

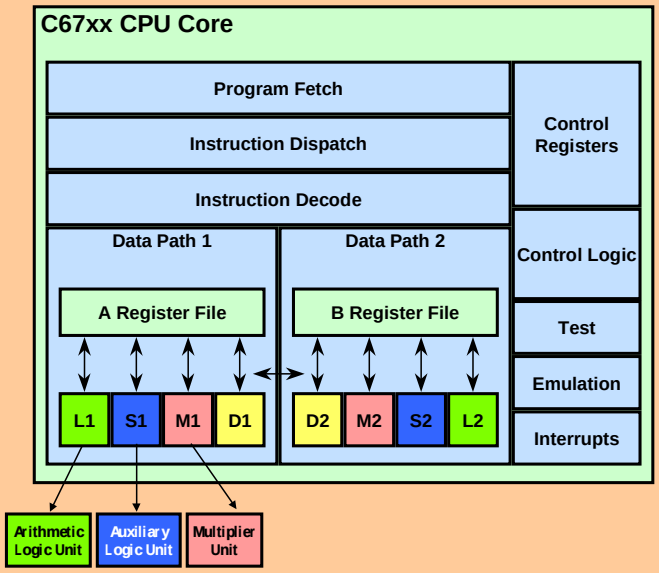
These highly orthogonal functional units provide code generation tools with many execution resources enabling these tools to maximize performance without extensive hand coding of assembly instructions by software developers. The C6701's instruction packing feature facilitates parallel instruction execution and supports instruction execution both in serial or in parallel/serial combinations. This optimized scheme enables significant reductions in code size, program fetches, and power consumption. All instructions can be conditional.

- Mirroring the C6201's core, the C6701's core includes 8-, 16- and 32-byte addressability; 8-bits of overflow protection; saturation; bit-field extract, set and clear; bit counting; normalization, and two additional integer multiply functional units with 32-bit and 16-bit multiply support.

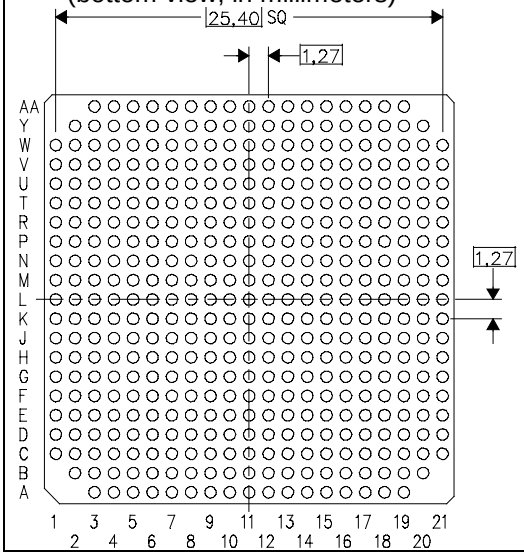
- 3.3-V peripherals on the chip including:
  - ✓ 1M-bit SRAM (½M dual access data RAM, ½M internal program RAM/cache)
  - ✓ 32-bit external memory interface (EMIF), glueless to SDRAM, SBSRAM, SRAM, EPROM
  - ✓ 4 channel DMA, bootloading direct memory access controller with an auxiliary channel
  - ✓ 2 multi-channel buffered serial ports (MCBSPS)
  - ✓ 2 32-bit general purpose timers
  - ✓ 16-bit flexible host port interface (HPI)
  - ✓ IEEE-1149.1 (JTAG) boundary scan compatible

CORE OVERVIEW

- 840 GFLOPS, 140 MHZ
  - 7-NS CYCLE TIME
  - 6, 32-BIT FLOATING-POINT INSTRUCTIONS PER CYCLE
- LOAD STORE ARCHITECTURE
- DUAL DATA PATHS
  - 8, 32-BIT INSTRUCTIONS/CYCLE
- IEEE FLOATING-POINT FORMAT
  - 840 MFLOPS SINGLE-PRECISION
  - 352 MFLOPS DOUBLE-PRECISION - HARDWARE SUPPORTED
  - DUAL DATA PATH
  - 8 FUNCTIONAL UNITS
- ADDITIONAL INTEGER MULTIPLY INSTRUCTIONS
  - NOT AVAILABLE ON THE C62X CORE
  - 32-BIT MULTIPLY
  - 16-BIT MULTIPLY
- INTEGER INSTRUCTION FEATURES
  - DATA BYTE ADDRESSABLE (8-, 16-, 32-BIT DATA)
  - 8-BITS OVERFLOW PROTECTION
  - SATURATION
  - BIT-FIELD EXTRACT, SET, CLEAR
  - BIT COUNTING
  - NORMALIZATION
- 32-BIT ADDRESS RANGE



C6701 PACKAGE INFORMATION

Package	Details
429-ceramic ball grid array (BGA) package (bottom view, in millimeters)  	27 x 27 mm package outline. This package requires less board area (a 40% area savings over a plastic 35 x 35 mm package). Ultra thin package (130 mils, 3.3 mm) supports military trend for higher integration and minimizing board space. 1.27 mm pitch on 46% Sn, 46% Pb, 8% Bi solderballs. Many edge solderballs will be no-connects and redundant V_{DD} and GNDs. These extra solder balls increase package-to-board reliability. Better thermal characteristics than most of the packages available on the market. Lower package cost passed on to customer.

DESIGN-IN SUPPORT

TI has the most extensive DSP application support

Product Information Center:	(972) 644-5580 (For general information, availability, etc.)
DSP Developer's Village	http://dspvillage.ti.com/docs/dspvillagehome.jhtml
DSP Hotline (Technical questions)	http://www.ti.com/sc/docs/dsps/hotline/support.htm
Third Parties URL	http://www.ti.com/sc/docs/general/dsp/third/index.htm
Military C6701 DSP Info	http://www.ti.com/sc/docs/products/military/processr/320c67x.htm
Ada Compiler	http://www.irvine.com

TECHNOLOGY

5-level metal CMOS process; ESD level = Category II (2,000 V to 3,999 V)
0.18-µm silicon, 140-MHz operation (167 MHz under evaluation), 1.8-V CPU core voltage
3.3-V on chip peripherals, all I/Os, memory, I/F, etc.

DIE SIZE

Die dimensions	11.2 x 11.2 mm (441 mils x 441 mils)
Die bond pad size	Circular bumps 80 µm in diameter
Die bond pad pitch	Variable from 225 µm to 275

POWER DISSIPATION

Maximum: 1.6 W for 0.18-µm silicon @ 140 MHz (est.)

PACKAGING

GLP = 429-ball C-DBGA Ceramic-Dimpled Ball Grid Array: A C-DBGA weighs 6.3 grams.

The following table and notes define the typical thermal characteristics for the ceramic GLP package. This data is useful for preliminary engineering evaluations.

PARAMETER	TYP	UNIT
$R_{\theta JA}$	14.47	°C/W
$R_{\theta JMA}$ (airflow@150 fpm)	11.79	°C/W
$R_{\theta JMA}$ (airflow@250 fpm)	11.09	°C/W
$R_{\theta JMA}$ (airflow@500 fpm)	10.21	°C/W
$R_{\theta JC}$ /1	7.34	°C/W
$R_{\theta JC}$ /2	3.00	°C/W
$R_{\theta JB}$	6.20	°C/W

Typical GLP Package Thermal Characteristics

Notes:

$R_{\theta JA}$	Junction-to-ambient air thermal resistance: measured in a one cubic foot, still air enclosure.
$R_{\theta JMA}$	Junction-to-moving air thermal resistance: measured in a wind tunnel.
$R_{\theta JC}$ /1	Junction-to-case thermal resistance: measured to the top of the package lid.
$R_{\theta JC}$ /2	Junction-to-case thermal resistance: measured to the bottom of solder ball.
$R_{\theta JB}$	Junction-to-board thermal resistance: measured by soldering a thermocouple to one of the middle traces on the board at the edge of the package.

The above values were obtained by mounting the 429-GLP on a FR-4 board and testing per JESD-51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages. The board design connected all the GND balls directly to a GND plane, V_{DD} balls to a V_{DD} plane, and all the signals were routed on the top layer.

Key features of the thermal test board design are:

- Board material: FR-4
- Board design: 2S2P (double layer, double buried power plane)
- Board thickness: 0.062 +/- 0.006 inches
- Board dimensions: 4.0 x 4.5 inches
- Trace thickness: 0.0028 inches
- Traces: 2 oz +/- 20% copper for signals and 1 oz +/- 10% copper for V_{DD} and GND planes

‘C6701 KEY FEATURES/BENEFITS

Key features	Benefits
Core compatible with the C620x fixed point processor	Facilitates reduced cycle-time development and eases transition between the C67x™ and C62x™ device families after the prototype phase. Also, supports flexible migration from C62 to C67x device families when the need for floating point calculations arise.
IEEE Floating Point Format	Double Precision - 4 cycle throughput Single Precision - Single cycle throughput
Advanced VLIW CPU with eight functional units (6 floating point / 2 fixed point) including two multipliers and six arithmetic units	Up to 10 times the performance of typical DSPs; Allows designers to develop highly effective RISC-like code for fast development time
Instruction packing	Code size equivalence for eight instructions executed serially or in parallel; Reduces code size, program fetches, and power consumption.
100 percent conditional instructions	Reduces costly branching; Increases parallelism for higher sustained performance.
Code executes as programmed on highly independent functional units	Benchmark suite and DSP industry's first assembly optimizer for fast development time.
8/16/32/64-bit data support	Efficient memory support for a variety of applications.
40-bit arithmetic options (32-bit store)	Extra precision for vocoders and other computationally intensive applications.
Bit-field manipulation and instruction: extract, set, clear, bit counting	Supports common operations found in control and data manipulation applications.
429-ceramic ball grid array (BGA) package. 27 x 27 mm package outline. 1.27 mm pitch	Ultra thin package supports military trend for higher integration and minimizing board space. Many Solderballs will be no-connects and redundant VDD and GNDs. These extra solder balls add additional package-to-board reliability. Less board area required (40% area savings over commercial 35 mm package). Better thermal characteristics than most of the packages available on the market. Lower package cost passed on to customer.
32-bit glueless external memory interface supports SDRAM, SBSRAM and SRAM	High speed connections to external memory for maximum sustained performance.
Two Multi-channel Buffered Serial Ports (McBSPs)	Glueless interface to high bandwidth telecommunications trunks; Provides high speed interprocessor communication
16-bit host access port	Host processor access to all memory (internal data memory, internal program memory, external memory).
Four data memory access (DMA) channels with bootloading capability	Efficient access to external memory/peripherals while minimizing CPU interrupts.
Flexible Phase-Locked-Loop (PLL) clock generator	Multiplies external clock rate by one or four for maximum CPU performance.

TEST VECTORS

The SM/SMJ320C6701 has ~2,000,000 test vectors. The test vectors are TI proprietary information.

PROCESS/PERFORMANCE OPTIONS

Device	Package	Speed	DSCC SMD	Processing
SN00372GLG Available Now	372-ball C-BGA	N/A	N/A	CBGA Daisy-Chain Package Prototype
SMJ320C6701GLPW14 Available Now	429-ball C-BGA	140 MHz	5962-9866101QXA	-55ºC to +115ºC Full Military QML Processing
SM320C6701GLPW14 Available Now	429-ball C-BGA	140 MHz	NA	-55ºC to +115ºC Extended Temp Processing
SM320C6701GLPS16 Available Now	429-ball C-BGA	167 MHz	N/A	-40ºC to +90ºC

NOMENCLATURE

SMJ **320** **C6701** **GLP** **W** **14**

SMJ = QML Process
SM = Commercial Process

320 = DSP Family

C6701 = Device

GLP = Package: GLP = Ceramic 429-Ball Grid Array

W = Extended (-55°C – 115°C)
S = Special Per Datasheet

14 = Speed: 14 = 140 MHz
16 = 167 MHz

TOOLS SUPPORT AND LITERATURE

A complete suite of C62x / C67x tools, just what programmers want. Contact your local TI authorized distributor for current pricing. Page 5 of the military C6000 Product Bulletin (http://www.ti.com/sc/docs/products/military/liter/sgub043a.pdf) contains additional information on tools availability, order numbers, and tool pricing.

Available Today:

- **C Compiler / Assembler / World's First Assembly Optimizer / and Linker**
  – TMDX3246855-07 for PC Win'95 and Win/NT
- **Software Simulator with software debugger**
  – TMDX3246851-07 for PC Win'95 and Win/NT
- **C Source Debugger with emulation S/W for hardware debug/emulation**
  – TMDX3240160-07 for PC Win'95 and Win/NT

IDE, fully **Integrated Development Environment** from GO-DSP **Available Now**
Code Composer Studio™ is the DSP industry's first fully integrated suite of software development tools for TI's C6000 DSPs. This advanced, open-DSP development environment provides designers with a real-time window into their target system and data enabled by seamless host-target communications and real-time debug and analysis capabilities. Code Composer Studio simplifies all aspects of the DSP development cycle by extending the capabilities of the Code Composer Integrated Development Environment (IDE) to encompass awareness of the DSP target by the host. For more information, please visit http://www.go-dsp.com/index.htm.

- **Hardware Emulator Controller Kit** :
  – TMDS00510 Emulator controller kit for PC
  The TMS320 family XDS-510 emulator is a user-friendly, PC-based development system which has all features necessary to perform full-speed, in circuit emulation with the TMS320C6000.
- **Evaluation Module (EVM) Board:** A low-cost PCI interfaced PC board which will include a C6701, SBSRAM, SDRAM, etc. is in development. It is well suited for software algorithm development.

Literature Information			**Literature Number**
Data sheets:	See Commercial data sheet on the web: sprs067d.pdf	(875 KB)	SPRS067
	See Military data sheet on the web: sgus030.pdf	(870 KB)	SGUS030

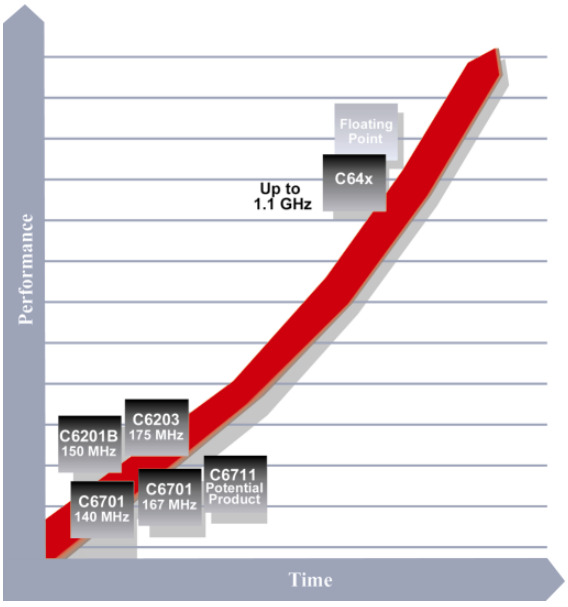
User Guides / User Manuals:

TMS320C6000	SOFTWARE TOOLS GETTING STARTED GUIDE	(364 KB)	SPRU185
TMS320C6X	ASSEMBLY LANGUAGE TOOLS USER'S GUIDE	(880 KB)	SPRU186
TMS320C6000	ASSEMBLY LANGUAGE TOOLS USER'S GUIDE	(2229 KB)	SPRU186
TMS320C6000	OPTIMIZING C COMPILER USER'S GUIDE	(1301 KB)	SPRU187
TMS320C6000	C SOURCE DEBUGGER	(1322 KB)	SPRU188
TMS320C62X/67X	CPU AND INSTRUCTION SET REFERENCE GUIDE	(879 KB)	SPRU189
TMS320C6201/C6701	PERIPHERALS REFERENCE GUIDE	(816 KB)	SPRU190
TMS320C62X/C67X	TECHNICAL BRIEF	(252 KB)	SPRU197
TMS320C62X/67X	PROGRAMMER'S GUIDE	(799 KB)	SPRU198
TMS320C6000	ADDENDUM TO TMS320 DSP DEV. SUPPORT REFERENCE GUIDE	(129 KB)	SPRU226
TMS320C6701	TEST AND EVALUATION BOARD TECHNICAL REF.	(1859 KB)	SPRU235
TMS320C6000	REV. EVALUATION MODULE REFERENCE GUIDE	(2603 KB)	SPRU269
TMS320C6000	PERIPHERAL SUPPORT LIBRARY PROGRAMMER'S REFERENCE	(430 KB)	SPRU273

COMMERCIAL HIGH PERFORMANCE ROADMAP

TI is has a migration path to higher performance floating point DSPs for the commercial market. These devices will be characterized for their extended temperature range performance capabilities.

SMJ320C6000 Military Roadmap

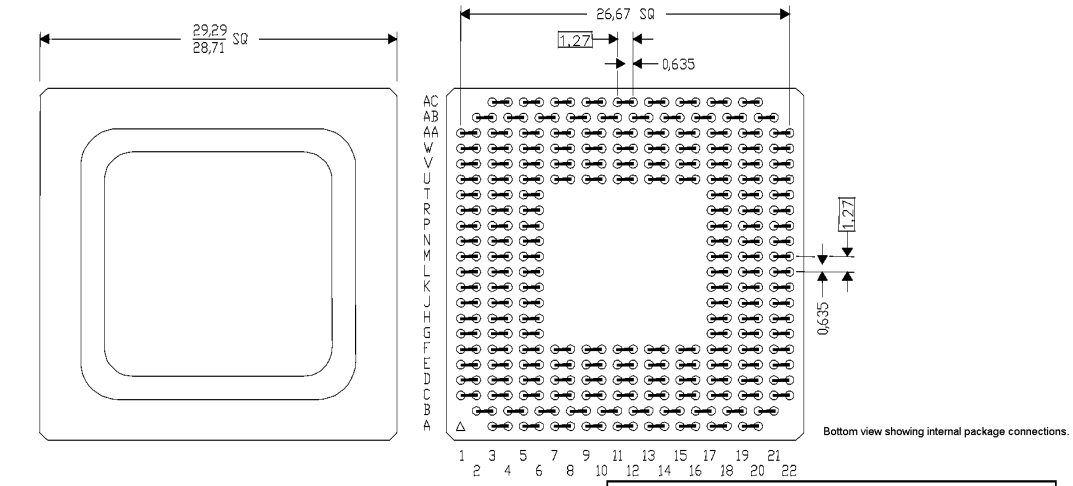


TEXAS INSTRUMENTS

Daisy Chain packages are used to evaluate/measure the package to board assembly process. They allow designers to verify the reliability of the package-to-board interface over temp cycles, shocks, aging, etc.

Daisy Chain CBGA (p/n=SN00372GLG)

for Ceramic-BGA to board Evaluation only



Notes: A All linear dimensions are in millimeters
B. This drawing is subject to change without notice

"GLG" and "GLP" Package Notes

D/C "GLG" package has 1.27 mm ball pitch same pitch as C6203 "GLP" package

D/C has Larger array size 22x22, not 21x21

D/C has Larger package 29mm Sq, not 27mm

Use of Daisy Chain

- **Internal to the D/C package, each Solderball is connected to one adjacent**
  Pattern: o-o o-o o-o o-o o-o o-o

- **The balls are linked to each other by a similar pattern on the D/C PCB evaluation board, thus forming one long chain connecting every solderball on the package. (PCB can also connect D/C package chain to another pkg.)**

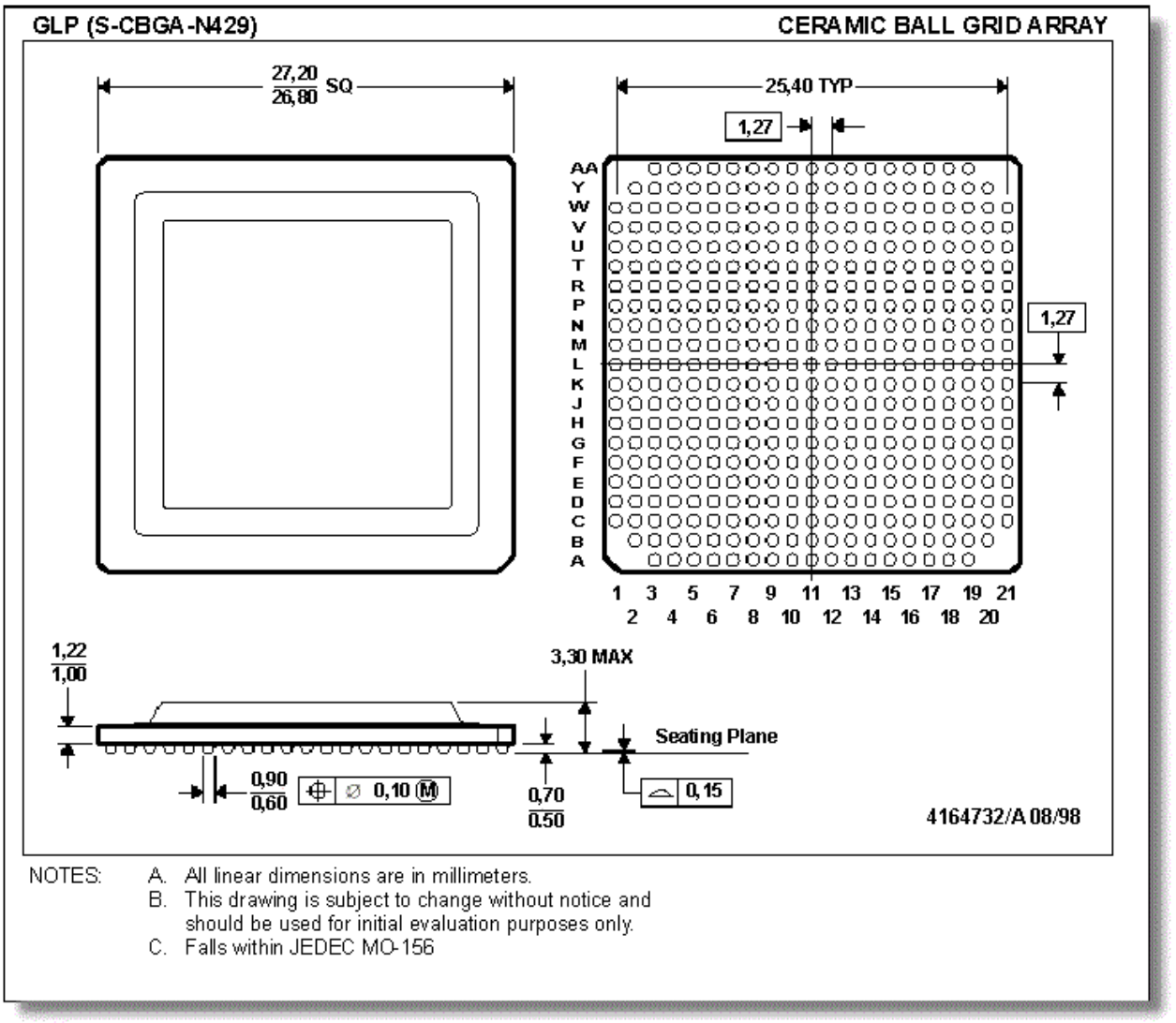
```
D/C Package Pattern:   o-o o-o o-o o-o o-o o-o
PCB Board Pattern:     o o=o o=o o=o o=o o=o o

Resulting Pattern:     o-o=o-o=o-o=o-o=o-o=o-o=o-o
                         (One long Chain)
```

- **Now, we can measure or monitor the continuity and resistance of all the D/C packages on an entire PCB (Every solderball of every package) by only two terminals.**

TEXAS INSTRUMENTS

The GLP package is used for the production versions of the ceramic ‘C6000 devices: 320C6201B and 320C6701.



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice and should be used for initial evaluation purposes only.
C. Falls within JEDEC MO-156

Test Socket Information

Q: Where can I find sockets for the ceramic versions of the C62x and C67x ?

A:
Test Sockets for 27x27 mm 1.27 mm pitch Ceramic Dimpled Ball Grid Array
High frequency test socket: which we use on our test boards:
Tecknit p/n 33-40028 we use on test boards tele: 908-272-5500
Description: "21x21x429 LGA test socket" ~$4K per socket.

Burn-In sockets: we are evaluating for use at 10MHz or less:
1. Tactic Electronics Inc., Distributor Dallas,TX 800-955-4707
   Tactic p/n:2441-8684-63-1902

2. Plastronics (Irvin TX) 972-258-1906
   p/n: 441BG12A127-D

The C6201BGLP and C6701GLP have identical pinouts and identical footprints.

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