Functional Safety Information

TPSM656x0
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for TPSM656x0 (WQFN-FCRLF (19) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

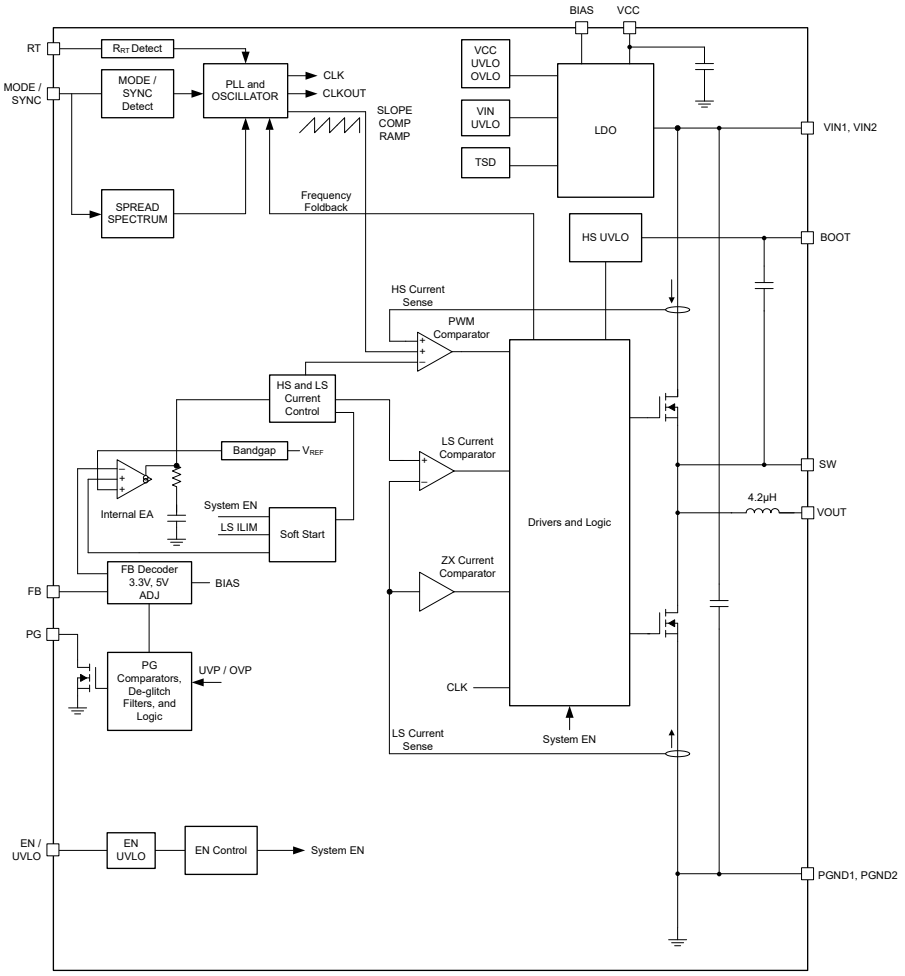

Figure 1-1. Functional Block Diagram

TPSM656x0 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 WQFN-FCRLF (19) Package

This section provides functional safety failure in time (FIT) rates for TPSM656x0 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	31
Die FIT rate	4
Package FIT rate	13
Passive FIT rate	14

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1.4W
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV > 50V supply	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPSM656x0 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	50
Output not in specification – voltage or timing	40
power FET stuck on	5
PGOOD false trip, fails to trip	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPSM656x0 (WQFN-FCRLF (19) package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-5 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The application circuit is implemented according to the TPSM656x0 data sheet

4.1 WQFN-FCRLF (19) Package

Figure 4-1 shows the TPSM656x0 pin diagram. For a detailed description of the device pins refer to the *Pin Configuration and Functions* section in the TPSM656x0 data sheet.

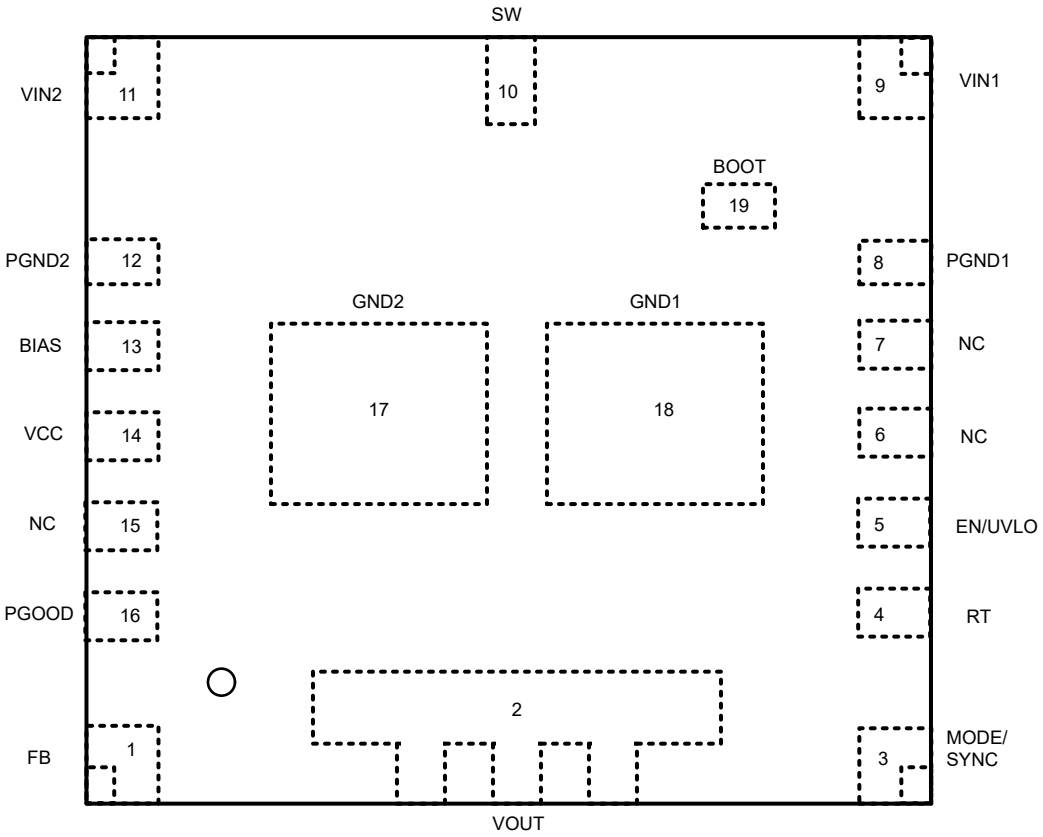

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
FB	1	If the pin is configured for the fixed 3.3Vout option, the FB pin shorts to ground by default. Normal operation.	D
		If the pin is configured for the fixed 5Vout option, the VCC pin shorts to ground. There is a loss of regulation.	B
		If the pin is configured for the adjustable output option, there is a loss of regulation. VOUT = VIN.	B
		If short happens at start-up, the device goes into the fixed 3.3Vout option.	B
VOUT	2	VOUT = 0V.	B
MODE/SYNC	3	There is no flag if configured for a PFM safe fault. The synchronize function is lost.	B
		The VCC pin shorts to ground if configured for a FPWM. VOUT = 0V.	B
RT	4	The VCC pin shorts to ground if the pin is configured for 400kHz. VOUT = 0V.	B
		There is a loss of regulation for the adjustable frequencies.	B
		The result is a safe fault if the pin is configured for 2.2MHz. Normal operation.	D
		If short happens at start-up, an unstable operation potentially occurs for the 2.2MHz configuration.	C
EN/UVLO	5	The device is disabled, VOUT = 0V.	B
NC	6	Normal operation.	D
	7		
	15		
PGND	8	Normal operation.	D
	12		
VIN	9	VOUT = 0V.	B
	11		
SW	10	The device is damaged.	A
BIAS	13	If the BIAS pin is tied to the VOUT pin, VOUT = 0V.	B
		If the BIAS pin is at ground, the result is a safe fault.	D
VCC	14	There is a loss of regulation. VOUT = 0V.	B
PGOOD	16	There is a loss of the power-good (PG) function.	B
GND	17	Normal operation.	D
	18		
BOOT	19	There is a loss of regulation, VOUT = 0V.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
FB	1	The next cycle is a non-switching cycle when the FB pin is configured for the fixed Vout option. PG is low.	C
		If open happens at start-up, there is no regulation. VOUT = 0V.	B
		If the FB pin is configured for the adjustable Vout option, VOUT = VIN.	B
VOUT	2	There is a loss of the power output.	B
MODE/SYNC	3	No flag; a PFM occurs in the next cycle. There is a loss of the external synchronize function.	B
RT	4	A PG low occurs in the next turn-on cycle for the 2.2MHz configuration.	C
		There is a loss of regulation for the adjustable frequencies, VOUT = 0V.	B
EN/UVLO	5	The device is disabled, VOUT = 0V.	B
NC	6	Normal operation.	D
	7		
	15		
PGND	8	Normal operation. There is a degradation in performance.	C
	12		
VIN	9	Normal operation. There is a degradation in performance.	B
	11		
SW	10	Normal operation.	D
BIAS	13	Normal operation.	D
VCC	14	The operation is unstable. No damage.	B
PGOOD	16	There is a loss of the power-good function.	B
GND	17	Normal operation. There is a degradation in performance.	C
	18		
BOOT	19	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FB	1	VOUT	The device is damaged if the VOUT pin is greater than the absolute maximum rating for the FB pin when a short occurs.	A
VOUT	2	MODE/SYNC	The device is damaged if the VOUT pin is greater than the absolute maximum rating for the MODE/SYNC pin when a short occurs.	A
MODE/SYNC	3	RT	The operation is normal when the RT and MODE pins are at ground.	D
			There is a loss of operation when the RT pin is at ground and the MODE pin is tied to VCC.	B
			The MODE pin is at VCC when the RT pin is populated with a resistor.	C
			There is a loss of operation when the RT pin is populated with a resistor and the MODE pin is at ground.	B
			At start-up, if the RT pin is populated with a resistor and the MODE pin is at VCC. An unstable operation potentially occurs during a 400kHz operation.	C
RT	4	EN/UVLO	There is a loss of regulation when the RT pin is populated with a resistor and enabled at the VIN pin.	B
			There is a loss of regulation when the RT pin is at ground and enabled at the VIN pin.	B
			There is damage to the device when the RT pin is tied to the VCC pin and enabled at the VIN pin.	A
EN/UVLO	5	NC	Normal operation.	D
NC	6	NC	Normal operation.	D
NC	7	PGND1	Normal operation.	D
PGND1	8	VIN1	VOUT = 0V.	B
VIN1	9	SW	There is damage to the device.	A
SW	10	VIN2	There is damage to the device.	A
VIN2	11	PGND2	VOUT = 0V.	B
PGND2	12	BIAS	The operation is normal if the BIAS pin is at ground.	D
			Hiccup mode occurs if the BIAS pin is tied to the VOUT pin.	B
			The operation is normal if the BIAS pin is floating.	D
BIAS	13	VCC	The BIAS pin is tied to the VOUT pin for the fixed Vout options. There is damage to the device if the VOUT pin is greater than the absolute maximum rating for the VCC pin when a short occurs.	A
VCC	14	NC	Normal operation.	D
NC	15	PGOOD	Normal operation.	D
PGOOD	16	FB	There is a loss of regulation when the FB pin is configured for the adjustable Vout options.	B
			There is a loss of the PG function when the FB pin is configured for the fixed Vout options.	C
			There is a loss of the PG function at start-up when the FB pin is configured for the fixed 3.3Vout option.	C
			PGOOD shorts VCC to ground at start-up if the FB pin is configured for the fixed 5Vout option.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
FB	1	There is damage to the device if the supply is > 5.5V.	A
VOUT	2	There is damage to the device if VIN > 24V.	A
MODE/SYNC	3	There is damage to the device if the supply is > 5.5V.	A
RT	4	The switching frequency is undefined.	C
EN/UVLO	5	Normal operation.	D
NC	6	Normal operation.	D
	7		
	15		
PGND	8	VOUT = 0V.	B
	12		
VIN	9	Normal operation.	D
	11		
SW	10	There is damage to the device.	A
BIAS	13	The device is potentially damaged if the input supply is greater than absolute maximum rating for the BIAS pin.	A
VCC	14	There is damage to the device if the supply is > 5.5V.	A
PGOOD	16	The device is potentially damaged if the input supply is greater than the absolute maximum rating for the PG pin.	A
GND	17	VOUT = 0V.	B
	18		
BOOT	19	There is damage to the device.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265