*Functional Safety Information*

# *TLV351x-Q1*
# *Functional Safety FIT Rate, FMD, and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for the following devices to aid in a functional safety system design:

| TLV3511-Q1 |
|---|
| SOT-23 (5) |
| SC70 (5) |

| TLV3512-Q1 |
|---|
| VSSOP (8) |

Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

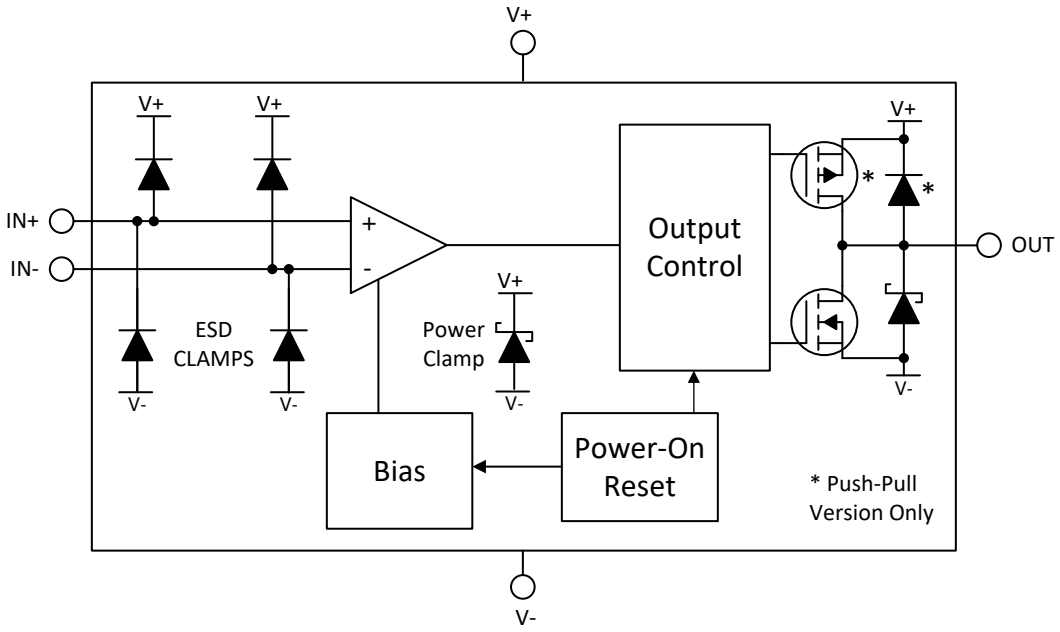


**Figure 1-1. Functional Block Diagram**

The TLV351x-Q1 family was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 SOT-23 (5) Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 (5) package of the TLV3511-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 4 |
| Die FIT rate | 2 |
| Package FIT rate | 2 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11 or figure 16
- Power dissipation: 10mW
- Climate type: world-wide table 8 or figure 13
- Package factor (lambda 3): table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 4 | Bipolar Op Amp, Comparators, Voltage Monitors | 12 FIT | 55 °C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 2.2 SC70 (5) Package

This section provides functional safety failure in time (FIT) rates for the SC70 (5) package of the TLV3511-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 3 |
| Die FIT rate | 2 |
| Package FIT rate | 1 |

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11 or figure 16
- Power dissipation: 10mW
- Climate type: world-wide table 8 or figure 13
- Package factor (lambda 3): table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 4 | Bipolar Op Amp, Comparators, Voltage Monitors | 12 FIT | 55 °C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 2.3 VSSOP (8) Package

This section provides functional safety failure in time (FIT) rates for the VSSOP (8) package of the TLV3512-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 6 |
| Die FIT rate | 2 |
| Package FIT rate | 4 |

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11 or figure 16
- Power dissipation: 10mW
- Climate type: world-wide table 8 or figure 13
- Package factor (lambda 3): table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 4 | Bipolar Op Amp, Comparators, Voltage Monitors | 12 FIT | 55 °C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLV351x-Q1 family in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| Out open (Hi-Z) | 15 |
| Out saturate high | 25 |
| Out saturate low | 25 |
| Out functional not in specification voltage or timing | 35 |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the TLV351x-Q1 device family. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to (V-) (see Table 4-2 and Table 4-6 )
- Pin open-circuited (see Table 4-3 and Table 4-7 )
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8 )
- Pin short-circuited to (V+) (see Table 4-5 and Table 4-9 )

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality. |
| B | No device damage, but loss of functionality. |
| C | No device damage, but performance degradation. |
| D | No device damage, no impact to functionality or performance. |

## 4.1 TLV3511-Q1 Packages

### *4.1.1 5-Pin Packages with OUT on Pin 1 (Northwest Pinout)*

Figure 4-1 shows the pin diagram for the TLV3511-Q1. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the data sheet.

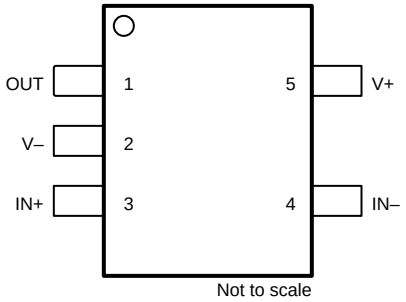


**Figure 4-1. Pin Diagram**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Negative Supply (V-) Pin**

| Pin Analysis for Pin Short-Circuit to Negative Supply (V-) | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **Device Damage** | **Device Functionality Affected** | **Description of Potential Failure Effects\|Comments** | **Failure Effect Class** |
| OUT | 1 | Potentially | Yes | Thermal stress due to high power dissipation | B |
| (V-) | 2 | No | No | No change if same node as (V-) | D |
| IN+ | 3 | No | No | Output goes low, if other input is positive | C |
| IN- | 4 | No | No | Output goes high, if other input is positive | C |
| (V+) | 5 | Potentially | Yes | Main supply shorted out (no power to device) | B |

**Table 4-3. Pin FMA for Device Pins Short-Circuited to Positive Supply (V+) Pin**

| Pin Analysis for Pin Short-Circuit to Positive Supply (V+) | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **Device Damage** | **Device Functionality Affected** | **Description of Potential Failure Effects\|Comments** | **Failure Effect Class** |
| OUT | 1 | Potentially | Yes | Thermal stress due to high power dissipation | B |
| (V-) | 2 | Potentially | Yes | Main supply shorted out (no power to device) | B |
| IN+ | 3 | No | No | Output goes high, if other input is less positive | C |
| IN- | 4 | No | No | Output goes low, if other input is less positive | C |
| (V+) | 5 | No | No | No change if same node as (V+) | D |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Analysis for Pin Short-Circuit to Adjacent Pin | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **Device Damage** | **Device Functionality Affected** | **Description of Potential Failure Effects\|Comments** | **Failure Effect Class** |
| OUT to (V-) | 1 → 2 | Potentially | Yes | Thermal stress due to high power dissipation | B |
| (V-) to IN+ | 2 → 3 | No | No | Output goes low, if other input is positive | C |
| IN+ to IN- | 3 → 4 | No | No | Output is potentially low or high | C |
| IN- to (V+) | 4 → 5 | No | No | Output goes low, if other input is less positive | C |
| (V+) to OUT | 5 → 1 | Potentially | Yes | Thermal stress due to high power dissipation | B |

**Table 4-5. Pin FMA for Device Pins Open-Circuited**

| Pin Analysis for Pin Open-Circuit | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **Device Damage** | **Device Functionality Affected** | **Description of Potential Failure Effects\|Comments** | **Failure Effect Class** |
| OUT | 1 | No | Yes | Output cannot drive application load | B |

**Table 4-5. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Analysis for Pin Open-Circuit | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **Device Damage** | **Device Functionality Affected** | **Description of Potential Failure Effects\|Comments** | **Failure Effect Class** |
| (V-) | 2 | Potentially | Yes | Lowest voltage pin drives GND pin internally (through a diode) | B |
| IN+ | 3 | No | No | Output is potentially low or high | C |
| IN- | 4 | No | No | Output is potentially low or high | C |
| (V+) | 5 | Potentially | Yes | Main supply open (no power to device) | B |

## 4.2 TLV3512-Q1 Packages

### *4.2.1 8-Pin Leaded Packages*

Figure 4-2 shows the pin diagram for the TLV3512-Q1. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the data sheet.

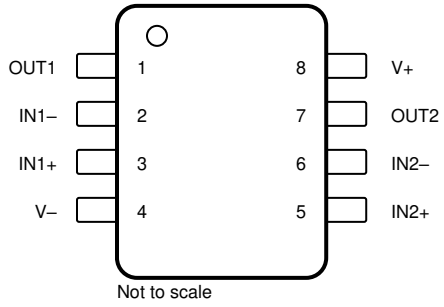


**Figure 4-2. Pin Diagram**

**Table 4-6. Pin FMA for Device Pins Short-Circuited to Negative Supply (V-) Pin**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| OUT1 | 1 | Thermal stress due to higher power dissipation | A |
| IN1- | 2 | OUT1 goes high if IN1+ is more positive | B |
| IN1+ | 3 | OUT1 goes low if IN1- is more positive | B |
| (V-) | 4 | Normal operation | D |
| IN2+ | 5 | OUT2 goes low if IN2- is more positive | B |
| IN2- | 6 | OUT2 goes high if IN2+ is more positive | B |
| OUT2 | 7 | Thermal stress due to higher power dissipation | A |
| (V+) | 8 | Main supply shorted out (no power to device) | B |

**Table 4-7. Pin FMA for Device Pins Short-Circuited to Positive Supply (V+) Pin**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| OUT1 | 1 | Thermal stress due to high power dissipation | A |
| IN1- | 2 | OUT1 goes low if IN1+ is less positive | B |
| IN1+ | 3 | OUT1 goes high if IN1- is less positive | B |
| (V-) | 4 | Main supply shorted out (no power to device) | B |
| IN2+ | 5 | OUT2 goes high if IN2- is less positive | B |
| IN2- | 6 | OUT2 goes low if IN2+ is less positive | B |
| OUT2 | 7 | Thermal stress due to high power dissipation | A |
| (V+) | 8 | No change (same node) | D |

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| OUT1 | 1 | IN1- | OUT1 is potentially high or low | B |
| IN1- | 2 | IN1+ | OUT1 is potentially high or low | B |
| IN1+ | 3 | (V-) | OUT1 goes low, if IN1- is more positive | B |
| (V-) | 4 | IN2+ | OUT2 goes low, if IN2- is more positive | B |
| IN2+ | 5 | IN2- | OUT2 is potentially high or low | B |
| IN2- | 6 | OUT2 | OUT2 is potentially high or low | B |

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| OUT2 | 7 | (V+) | Thermal stress due to higher power dissipation | A |
| (V+) | 8 | OUT1 | Thermal stress due to higher power dissipation | A |

**Table 4-9. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| OUT1 | 1 | OUT1 cannot drive application load or toggle high | B |
| IN1- | 2 | OUT1 is potentially high or low | B |
| IN1+ | 3 | OUT1 is potentially low or high | B |
| (V-) | 4 | Lowest voltage pin drives (V-) pin internally (through a diode) | B |
| IN2+ | 5 | OUT2 is potentially high or low | B |
| IN2- | 6 | OUT2 is potentially high or low | B |
| OUT2 | 7 | OUT2 cannot drive application load or toggle high | B |
| (V+) | 8 | Main supply open (no power to device) | B |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| May 2025 | * | Initial Release |

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265