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1 Overview

This document contains information for HDC3120-Q1 (SOT563-6 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

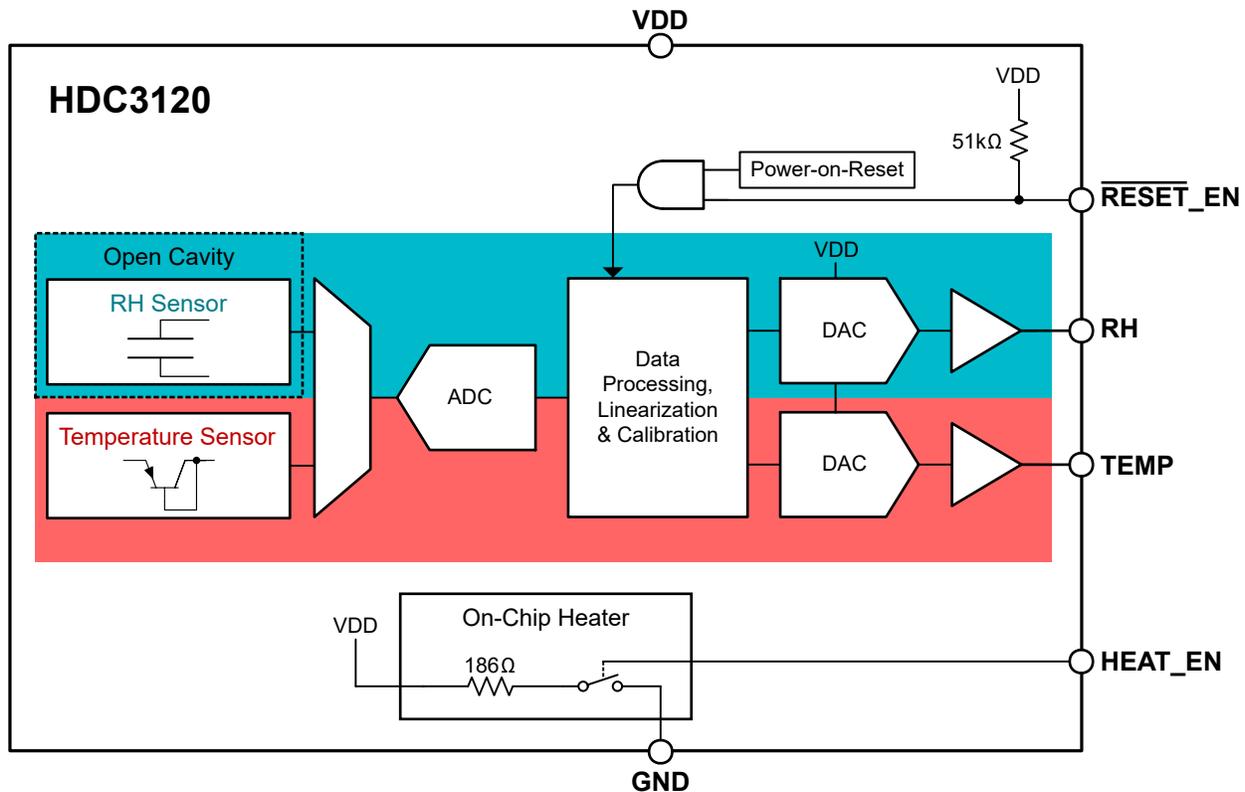


Figure 1-1. Functional Block Diagram

HDC3120-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for HDC3120-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	5
Die FIT rate	2
Package FIT rate	3

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 2.73mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Note

Assumes the HDC3120 on-chip heater is enabled for ten minutes daily.

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for HDC3120-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
RH output or TEMP output is incorrect and out of specification	65
RH output or TEMP output oscillating and unstable	25
Device not powering on correctly	5
RESET_EN asserts incorrectly	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the HDC3120-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the HDC3120-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the HDC3120-Q1 data sheet.

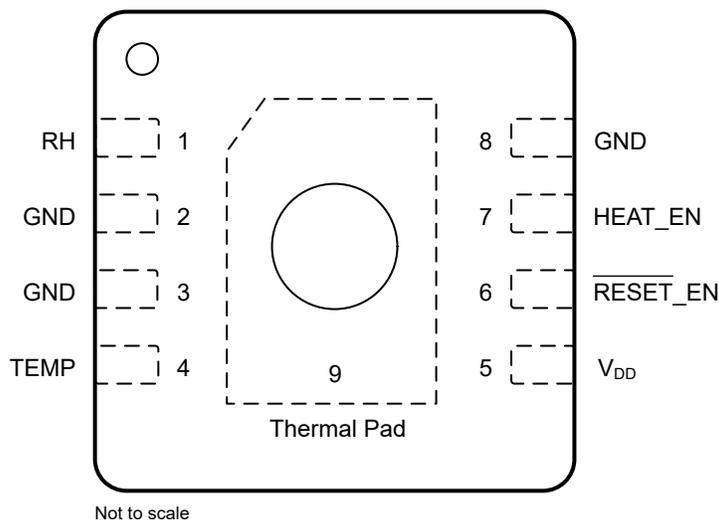


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is the only target on the I2C bus
- External pull-up resistor on SCL and SDA pins

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RH	1	RH stuck low, not functional, not possible to read the RH voltage output.	B
GND	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
TEMP	4	TEMP stuck low, not functional, not possible to read the TEMP voltage output.	B
VDD	5	Device not powered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RESET_EN	6	RESET_EN stuck low, RESET_EN is permanently enabled, device non-functional until reset is cleared.	B
HEAT_EN	7	HEAT_EN stuck low, the heater is not able to be turned on, the heater is the only function lost.	B
GND	8	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RH	1	Reading the RH output is impossible.	B
GND	2	Device functionality is undetermined. Device potentially does not power or connect to ground internally through the alternate pin ESD diode and power up.	B
GND	3	Device functionality is undetermined. Device potentially does not power or connect to ground internally through alternate pin ESD diode and power up.	B
TEMP	4	Reading the TEMP output is impossible.	B
VDD	5	Device functionality is undetermined. Device not powered if all external analog and digital pins are held low. Device can power up through the internal ESD diodes to VDD, if voltages above the power-on reset threshold for the device are present on any of the analog or digital pins.	B
RESET_EN	6	RESET_EN can inadvertently trigger if the floating input voltage clears the VIH threshold, resetting the device.	B
HEAT_EN	7	HEAT_EN can trigger the heater to inadvertently turn on if the floating input voltage clears the VIH threshold.	B
GND	8	Device functionality is undetermined. Device potentially does not power or connect to ground internally through alternate pin ESD diode and power up.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RH	1	GND	RH stuck low, not functional, not possible to read the RH voltage output.	B
GND	2	GND	No effect. Normal operation.	D
GND	3	TEMP	TEMP stuck low, not functional, not possible to read the TEMP voltage output.	B
VDD	5	RESET_EN	RESET_EN stuck high, cannot issue resets with nRESET pin.	B
RESET_EN	6	HEAT_EN	Heater enables when reset is not triggered and reset triggers when the heater is disabled. Leads to inadvertent heater activation and reset events, loss of functionality.	B
HEAT_EN	7	GND	HEAT_EN stuck low, the heater is not able to be turned on, the heater is the only function lost.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RH	1	RH stuck high, not functional, not possible to read the RH voltage output.	B
GND	2	Device functionality is undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
GND	3	Device functionality is undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A
TEMP	4	TEMP stuck high, not functional, not possible to read the TEMP voltage output.	B
VDD	5	No effect. Normal operation.	D
RESET_EN	6	RESET_EN stuck high, cannot issue resets with the RESET_EN pin.	B
HEAT_EN	7	HEAT_EN stuck high, the heater is permanently enabled, degrades performance and accuracy of the RH and TEMP outputs.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	8	Device functionality is undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is plausible.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial Release

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