Functional Safety Information

TLV9152-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TLV9152-Q1 (VSSOP (DGK) | 8, SOIC (D) | 8, and TSSOP (PW) | 8 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

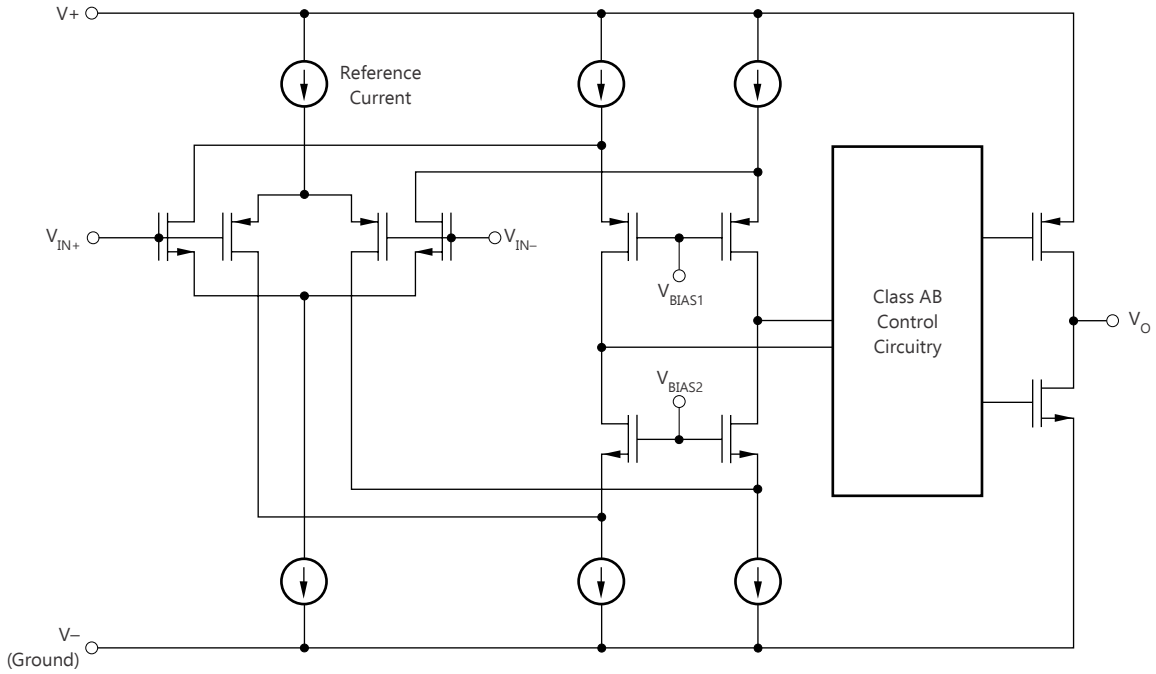

Figure 1-1. Functional Block Diagram

The TLV9152-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSSOP (DGK) | 8 Package

This section provides functional safety failure in time (FIT) rates for the VSSOP (DGK) | 8 package of the TLV9152-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	3
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 10.96mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOIC (D) | 8 Package

This section provides functional safety failure in time (FIT) rates for the SOIC (D) | 8 package of the TLV9152-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	3
Package FIT rate	7

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 10.96mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 TSSOP (PW) | 8 Package

This section provides functional safety failure in time (FIT) rates for the TSSOP (PW) | 8 package of the TLV9152-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	3
Package FIT rate	6

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 10.96mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLV9152-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20
Output saturate high	25
Output saturate low	25
Output functional, not in specification voltage or timing	30

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLV9152-Q1 (VSSOP (DGK) | 8, SOIC (D) | 8, and TSSOP (PW) | 8 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2, Table 4-6, and Table 4-10)
- Pin open-circuited (see Table 4-3, Table 4-7, and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, and Table 4-12)
- Pin short-circuited to supply (see Table 4-5, Table 4-9, and Table 4-13)

Table 4-2 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Short circuit to power means short to V+
- Short circuit to GND and short circuit to ground mean short to V–
- V+ is equivalent to VCC
- V– is equivalent to VEE

4.1 VSSOP (DGK) | 8 Package

Figure 4-1 shows the TLV9152-Q1 pin diagram for the VSSOP (DGK) | 8 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLV9152-Q1 data sheet.

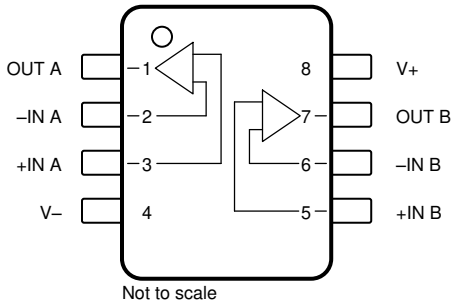

Figure 4-1. Pin Diagram (VSSOP (DGK) | 8) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
–IN A	2	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN B	5	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
–IN B	6	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	8	Op amp supplies are shorted together, leaving the V+ pin at some voltage between the V+ and V– sources (depending on the source impedance).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	No negative feedback or ability for OUT A to drive the application.	B
–IN A	2	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
+IN A	3	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
V–	4	Negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
+IN B	5	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
–IN B	6	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
OUT B	7	No negative feedback or ability for OUT B to drive the application.	B
V+	8	Positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	2	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	B
–IN A	2	3	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
+IN A	3	4	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
V–	4	5	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN B	5	6	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
–IN B	6	7	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	`B
OUT B	7	8	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	8	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the V+ voltage ultimately forced to the OUT A voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
–IN A	2	The device does not receive negative feedback. Depending on the non-inverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to +IN A.	B
V–	4	Op-amp supplies are shorted together, leaving the V– pin at some voltage between the V– and V+ sources (depending on the source impedance).	A
+IN B	5	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to +IN B.	B
–IN B	6	The device does not receive negative feedback. Depending on the non-inverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

4.2 SOIC (D) | 8 Package

Figure 4-2 shows the TLV9152-Q1 pin diagram for the SOIC (D) | 8 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLV9152-Q1 data sheet.

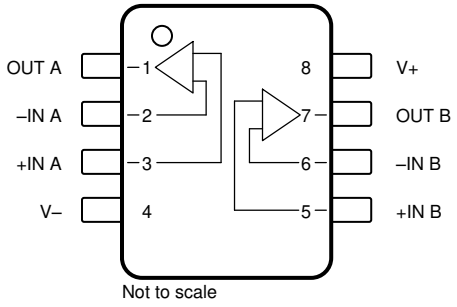

Figure 4-2. Pin Diagram (SOIC (D) | 8 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
–IN A	2	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN B	5	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
–IN B	6	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	8	Op-amp supplies are shorted together, leaving the V+ pin at some voltage between the V+ and V– sources (depending on the source impedance).	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	No negative feedback or ability for OUT A to drive the application.	B
–IN A	2	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
+IN A	3	Device common–mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
V–	4	Negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
+IN B	5	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
–IN B	6	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
OUT B	7	No negative feedback or ability for OUT B to drive the application.	B
V+	8	Positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	2	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application not functioning as intended is possible.	B
–IN A	2	3	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
+IN A	3	4	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
V–	4	5	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN B	5	6	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
–IN B	6	7	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application not functioning as intended is possible.	B
OUT B	7	8	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	8	1	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the V+ voltage ultimately forced to the OUT A voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
–IN A	2	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Depending on the circuit configuration, the application is likely not to function because device common–mode voltage is connected to +IN A.	B
V–	4	Op-amp supplies are shorted together, leaving the V– pin at some voltage between the V– and V+ sources (depending on the source impedance).	A
+IN B	5	Depending on the circuit configuration, the application is likely not to function because device common–mode voltage is connected to +IN B.	B
–IN B	6	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

4.3 TSSOP (PW) | 8 Package

Figure 4-3 shows the TLV9152-Q1 pin diagram for the TSSOP (PW) | 8 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLV9152-Q1 data sheet.

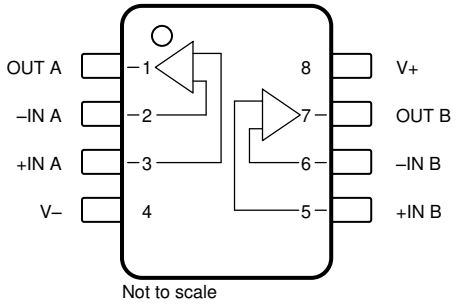

Figure 4-3. Pin Diagram (TSSOP (PW) | 8 Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
–IN A	2	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN B	5	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
–IN B	6	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	8	Op-amp supplies are shorted together, leaving the V+ pin at some voltage between the V+ and V– sources (depending on the source impedance).	A

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	No negative feedback or ability for OUT A to drive the application.	B
–IN A	2	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
+IN A	3	Device common–mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
V–	4	Negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
+IN B	5	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
–IN B	6	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
OUT B	7	No negative feedback or ability for OUT B to drive the application.	B
V+	8	Positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	A

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	2	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application not functioning as intended is possible.	B
–IN A	2	3	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
+IN A	3	4	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
V–	4	5	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN B	5	6	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
–IN B	6	7	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application not functioning as intended is possible.	B
OUT B	7	8	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	8	1	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the V+ voltage ultimately forced to the OUT A voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

Table 4-13. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
–IN A	2	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Depending on the circuit configuration, the application is likely not to function because device common–mode voltage is connected to +IN A.	B
V–	4	Op-amp supplies are shorted together, leaving the V– pin at some voltage between the V– and V+ sources (depending on the source impedance).	A
+IN B	5	Depending on the circuit configuration, the application is likely not to function because device common–mode voltage is connected to +IN B.	B
–IN B	6	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

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