Functional Safety Information

TPS2HCS08-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPS2HCS08-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagram for reference.

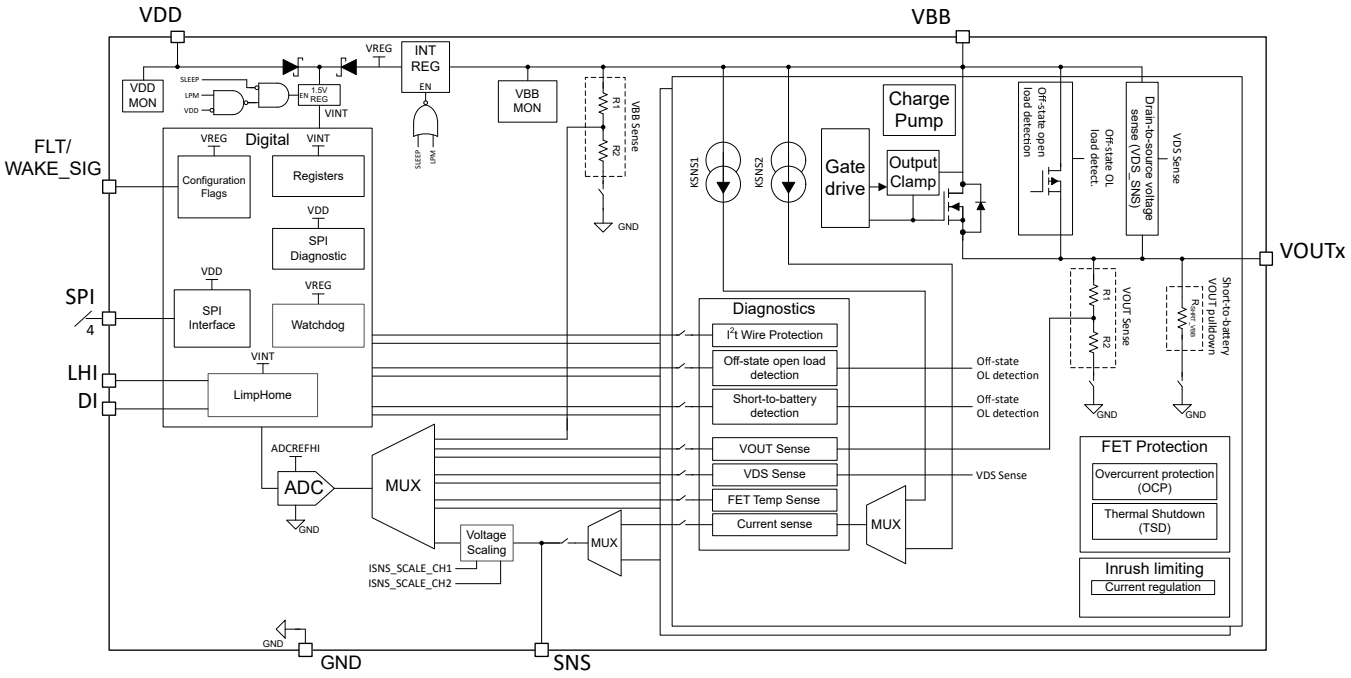

Figure 1-1. TPS2HCS08A-Q1 Functional Block Diagram

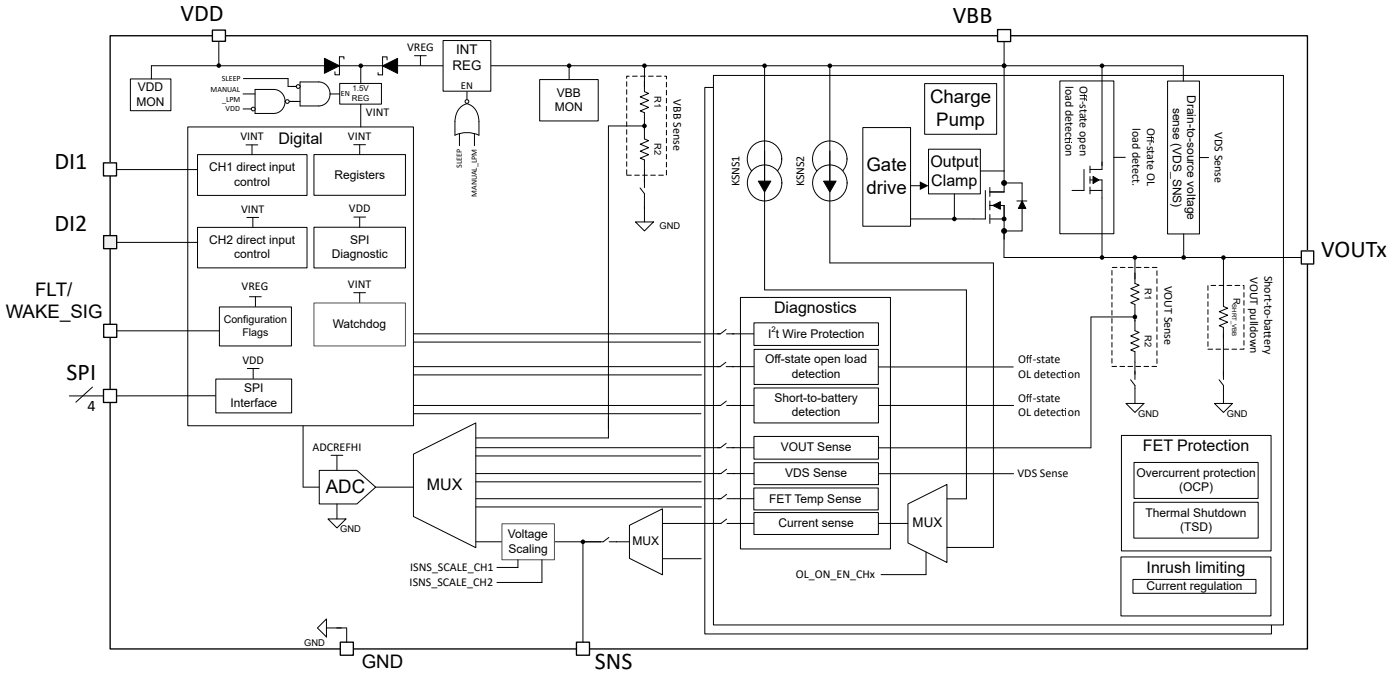

Figure 1-2. TPS2HCS08B-Q1 Functional Block Diagram

TPS2HCS08-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS2HCS08-Q1 based on the industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	15
Die FIT rate	5
Package FIT rate	10

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS2HCS08-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	20
VOUT stuck on (VBB)	10
VOUT functional, not within specification (voltage or timing)	50
Diagnostics not in specification	10
Protect functions fail to trip	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS2HCS08-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

The following figures show the TPS2HCS08-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS2HCS08-Q1 data sheet.

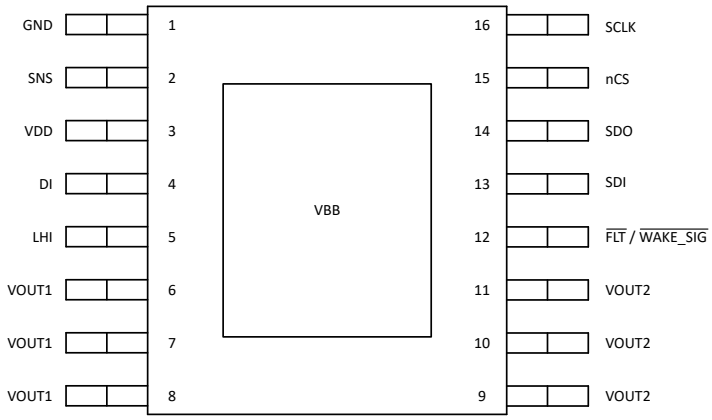

Figure 4-1. Pin Diagram Version A

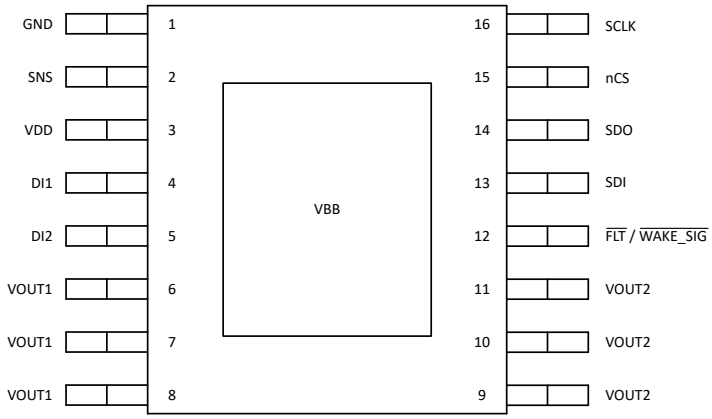

Figure 4-2. Pin Diagram Version B

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follow the data sheet recommendations for operating conditions, external component selection, and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Resistor or diode network is bypassed if present.	B
SNS	2	SNS current diagnostics (including I2T if enabled) are not available.	B
VDD	3	SPI communication is non-functional.	B
DI (version A)	4	Output control might be lost in LIMP_HOME state if CHx_LH_IN = 00, otherwise, no effect.	B
DI1 (version B)	4	Channel 1 is disabled.	B
LHI (version A)	5	Device is not able to enter in LIMP_HOME state through LHI input.	B
DI2 (version B)	5	Channel 2 is disabled.	B
VOUT1	6	Short to GND protection starts to protect channel 1.	B
	7		
	8		
VOUT2	9	Short to GND protection starts to protect channel 2.	B
	10		
	11		
$\overline{\text{FLT/WAKE\_SIG}}$	12	Fault indication can be incorrect. Fault indication and LPM wake-up indication cannot be reported to the MCU through the $\overline{\text{FLT/WAKE\_SIG}}$ pin.	B
SDI	13	SPI communication is non-functional.	B
SDO	14	Cannot use SPI to read faults and diagnostics. Verify that the R_{VDD} resistor is available to limit the short-circuit current.	B
CSN	15	SPI communication is non-functional.	B
SCLK	16	SPI communication is non-functional.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Loss of ground detection engages and the device turns off channels. **Note**: Loss of ground detection engages if $R_{SDO} \geq 768\Omega$.	B
SNS	2	SNS current diagnostics (including I2T if enabled) are not available.	B
VDD	3	SPI communication is non-functional.	B
DI (version A)	4	Output control might be lost in LIMP_HOME state if CHx_LH_IN = 00, otherwise, no effect. DI is pulled down internally.	B
DI1 (version B)	4	Channel 1 is disabled. DI1 is pulled down internally.	B
LHI (version A)	5	Device is not able to enter in LIMP_HOME state through LHI input. LHI is pulled down internally.	B
DI2 (version B)	5	Channel 2 is disabled. DI2 is pulled down internally.	B
VOUT1	6	No effect. If off-state open load detection is configured, open load detection is triggered when channel 1 is disabled.	C
	7		
	8		
VOUT2	9	No effect. If off-state open load detection is configured, open load detection is triggered when channel 2 is disabled.	C
	10		
	11		
$\overline{\text{FLT/WAKE\_SIG}}$	12	Fault indication can be incorrect. Fault indication and LPM wake-up indication cannot be reported to the MCU through the $\overline{\text{FLT/WAKE\_SIG}}$ pin.	B
SDI	13	SPI communication is non-functional.	B
SDO	14	Cannot use SPI to read faults and diagnostics.	B
CSN	15	SPI communication is non-functional.	B
SCLK	16	SPI communication is non-functional.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	2 (SNS)	SNS current diagnostic is not available.	B
SNS	2	3 (VDD)	Sense output can be incorrect. SPI communication is non-functional.	B
VDD	3	4 (DI)	Output control might be lost in LIMP_HOME state if CHx_LH_IN = 00, otherwise, no effect to the output control of the device. SPI communication is non-functional.	B
VDD	3	4 (DI1)	Channel 1 output control might be lost.	B
DI	4	5 (LHI)	Output control might be lost in LIMP_HOME state if CHx_LH_IN = 00, otherwise, no effect to the output control of the device. Might not be able to enter LIMP_HOME state through the LHI pin.	B
DI1	4	5 (DI2)	Channel 1 or Channel 2 (or both) output control might be lost.	B
LHI	5	6 (VOUT1)	Device might not able to enter in LIMP_HOME state through the LHI input.	B
DI2	5	6 (VOUT1)	Channel 2 output control might be lost.	B
VOUT2	11	12 ($\overline{\text{FLT}}$/ $\overline{\text{WAKE\_SIG}}$)	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit. Fault indication can be incorrect. Fault indication and LPM wake-up indication cannot be reported to the MCU through the $\overline{\text{FLT/WAKE\_SIG}}$ pin.	A
$\overline{\text{FLT/WAKE\_SIG}}$	12	13 (SDI)	Fault indication and LPM wake-up indication can be incorrectly reported to the MCU through the $\overline{\text{FLT/WAKE\_SIG}}$ pin. SPI communication is non-functional.	B
SDI	13	14 (SDO)	SPI communication is non-functional.	B
SDO	14	15 (CSN)	SPI communication is non-functional.	B
CSN	15	16 (SCLK)	SPI communication is non-functional.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Supply power is bypassed and the device does not turn on.	B
SNS	2	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
VDD	3	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
DI	4	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
DI1	4	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
LHI	5	Device is not able to enter in LIMP_HOME state through the LHI input.	B
DI2	5	Channel 2 output control might be lost.	B
VOUT1	6	Output shorted to supply. If off-state short-to-battery detection is configured, short-to-battery detection is triggered when channel 1 is disabled.	B
	7		
	8		
VOUT2	9	Output shorted to supply. If off-state short-to-battery detection is configured, short-to-battery detection is triggered when channel 2 is disabled.	B
	10		
	11		
$\overline{\text{FLT/WAKE\_SIG}}$	12	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit. Fault indication and LPM wake-up indication can be incorrectly reported to the MCU through the $\overline{\text{FLT/WAKE\_SIG}}$ pin.	A
SDI	13	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
SDO	14	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
CSN	15	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SCLK	16	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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