Functional Safety Information

LM5190 and LM25190
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM5190 and LM25190 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

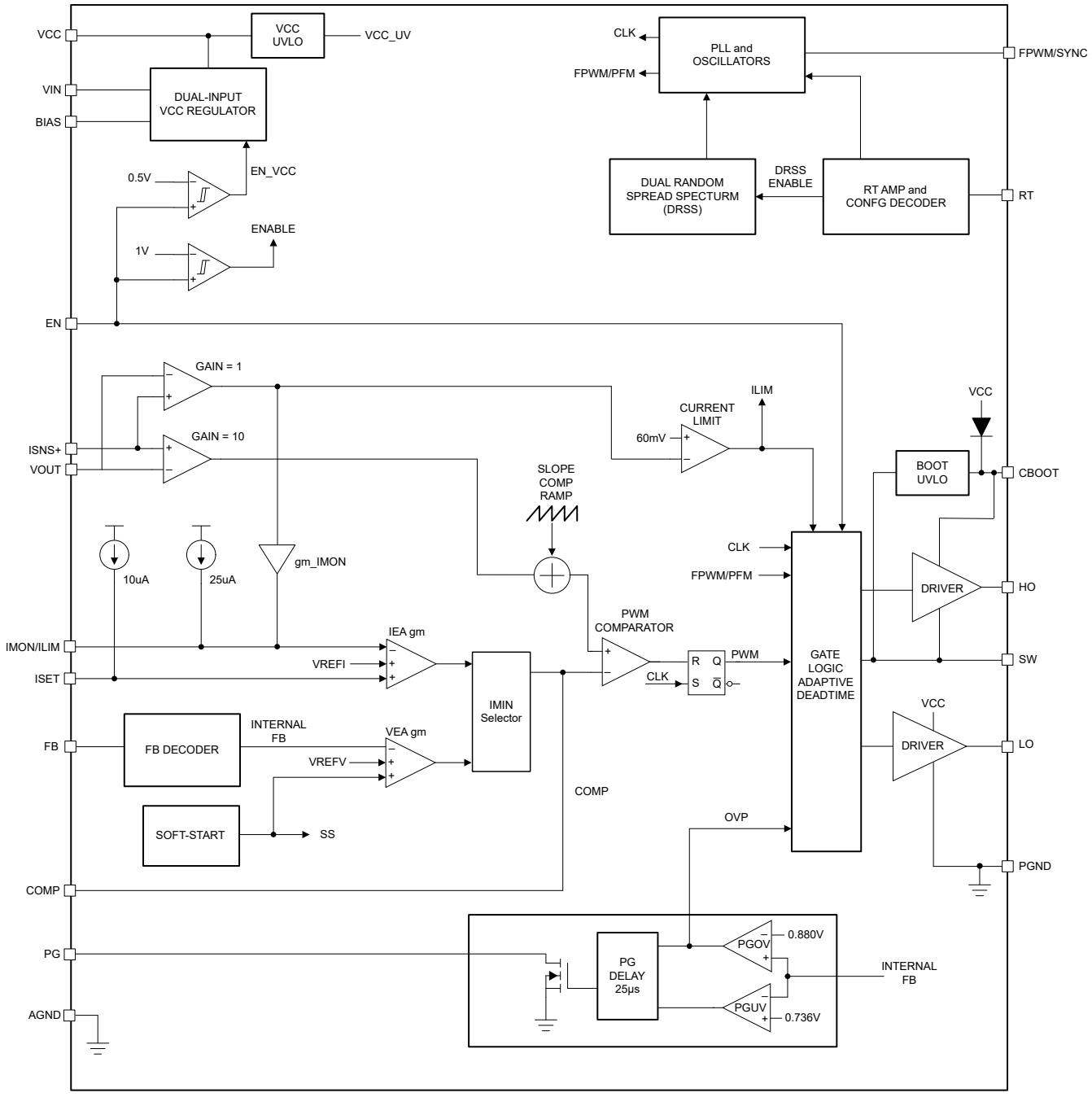

Figure 1-1. Functional Block Diagram

LM5190 and LM25190 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM5190 and LM25190 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	7
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 750mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV > 50V supply	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5190 and LM25190 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	40
Output not in specification – voltage or timing	25
Gate driver stuck on	5
Constant – current limit not in specification	20
Power good – false trip or fails to trip	5
Short circuit any two pins	5

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5190 and LM25190. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM5190 and LM25190 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM5190 and LM25190 data sheets.

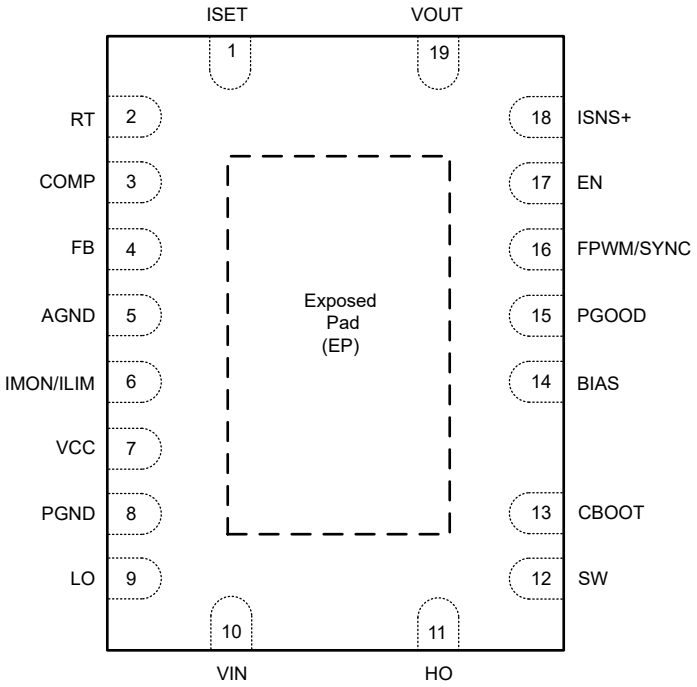

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	VOUT = 0V. ISET is not functional.	B
RT	2	VOUT attempts to regulate at maximum fsw, causing maximum power dissipation.	C
COMP	3	VOUT = 0V.	B
FB	4	VOUT target set to 5V.	B
AGND	5	AGND is GND. VOUT = expected VOUT.	D
IMON/ILIM	6	VOUT = expected VOUT. Current monitor and CC limit are not functional.	B
VCC	7	VOUT = 0V, no switching, loaded VCC output.	B
PGND	8	PGND is GND. VOUT = expected VOUT.	D
LO	9	VOUT = 0V, the VCC regulator is loaded to current limit.	B
VIN	10	VOUT = 0V.	B
HO	11	VOUT = 0V, the VCC regulator is loaded to current limit.	B
SW	12	VOUT = 0V. High-side FET is shorted from VIN to GND.	A
CBOOT	13	VOUT = 0V. High-side FET is shorted from VIN to GND.	B
BIAS	14	VOUT = expected VOUT. Internal VCC regulator provides bias voltage.	C
PGOOD	15	VOUT = expected VOUT. PGOOD is not functional.	C
FPWM/SYNC	16	VOUT = expected VOUT. No synchronization is available and always in PFM mode.	C
EN	17	VOUT = 0V. Always in shutdown.	B
ISNS+	18	VOUT = 0V.	A
VOUT	19	VOUT = 0V.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	VOUT = expected VOUT. ISET is not functional.	C
RT	2	RT regulates to 1V, but the internal oscillator does not function.	B
COMP	3	VOUT oscillates.	A
FB	4	VOUT = VIN.	A
AGND	5	VOUT is indeterminate.	B
IMON/ILIM	6	VOUT = 0V. Current monitor and CC limit are not functional.	B
VCC	7	VOUT = 0V.	B
PGND	8	VOUT = 0V.	B
LO	9	VOUT = expected VOUT with reduced efficiency.	C
VIN	10	VOUT = 0V.	B
HO	11	If HO is opened while HO to SW has voltage, the high-side FET never turns off. VOUT = VIN.	A
SW	12	VOUT is indeterminate. The CBOOT floating rail has no reference to the actual SW node. VOUT = VIN.	A
CBOOT	13	VOUT = 0V.	B
BIAS	14	VOUT = expected VOUT. Internal VCC regulator provides bias voltage.	C
PGOOD	15	VOUT = expected VOUT. PGOOD is not functional.	C
FPWM/SYNC	16	VOUT = expected VOUT. No synchronization is available and always in FPWM mode.	C
EN	17	VOUT = 0V.	B
ISNS+	18	The open ISNS+ pin blocks current limit and causes VOUT oscillations.	A
VOUT	19	VOUT = 0V, if the internal feedback is used.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ISET	1	RT	If RT resistor is tied to VCC, ISET pin can be damaged. If RT resistor is tied to AGND, VOUT = expected VOUT. The switching frequency is lower. CC operation is affected.	A
RT	2	COMP	If RT resistor is tied to VCC, COMP pin can be damaged. If RT resistor is tied to AGND, VOUT = 0V.	A
COMP	3	FB	External FB mode: COMP regulates to 0.8V and output is unregulated. VOUT = indeterminate.	B
			Internal FB mode FB = VCC, device is damaged.	A
			Internal FB mode FB = GND, VOUT = 0V.	B
FB	4	AGND	VOUT target set to 5V.	B
AGND	5	IMON/ILIM	VOUT = expected VOUT. Current monitor and CC limit are not functional.	C
IMON/ILIM	6	VCC	Device damage.	A
VCC	7	PGND	VCC is grounded. VOUT = 0V.	B
PGND	8	LO	VOUT = 0V. VCC is loaded by the LO driver.	B
LO	9	VIN	VOUT = 0V. The driver is damaged if VIN > 8V.	A
VIN	10	HO	For VIN > 8V, exceeds the maximum ratings and the HO pin is damaged. For VIN < 8V, VOUT = dropout lower than VIN, no switching, and excess current from VIN.	A
HO	11	SW	VOUT = 0V.	B
SW	12	CBOOT	VOUT = 0V.	B
CBOOT	13	BIAS	Device damage if CBOOT > 30V.	A
BIAS	14	PGOOD	PG pulldown can damage. VOUT = expected VOUT.	A
PGOOD	15	FPWM/SYNC	VOUT = expected VOUT. If FPWM is tied to VCC, PG pulldown can be damaged.	A
FPWM/SYNC	16	EN	VOUT = expected VOUT.	A
EN	17	ISNS+	EN is high-voltage rated. VOUT = expected VOUT if VOUT > 1V. If VOUT < 1V, the device is disabled.	B
ISNS+	18	VOUT	Current limit is disabled since the current limit resistor is shorted. VOUT cannot regulate since current-mode feedback is shorted.	A
VOUT	19	ISET	VOUT = 0V. If prebias VOUT > 5.5V, ISET pin is damaged.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	Device damage if VIN > 5.5V.	A
RT	2	Device damage if VIN > 8V.	A
COMP	3	Device damage if VIN > 5.5V If VIN < 5.5V, VOUT out of regulation.	A
FB	4	Device damage if VIN > 8V. If VIN < 8V, VOUT = VIN.	A
AGND	5	VOUT = 0V.	B
IMON/ILIM	6	Device damage if VIN > 5.5V.	A
VCC	7	Device damage if VIN > 8V. If VIN < 8V, VOUT = expected VOUT.	A
PGND	8	VOUT = 0V.	B
LO	9	VOUT = 0V. The driver is damaged if VIN > 8V.	A
VIN	10	N/A	D
HO	11	For VIN > 8V, exceeds maximum ratings and the HO pin is damaged For VIN < 8V, VOUT = dropout lower than VIN, no switching, and excess current from VIN	A
SW	12	VOUT = VIN, excess current from VIN. LO turns on and shorts against VIN.	B
CBOOT	13	Device damage if VIN > 8V. If VIN < 8V, VOUT < expected VOUT.	A
BIAS	14	Device damage if VIN > 30V.	A
PGOOD	15	Device damage.	A
FPWM/SYNC	16	Device damage if VIN > 8V. If VIN < 8V, VOUT = expected VOUT but always FPWM mode.	A
EN	17	Always on. VOUT = expected VOUT.	C
ISNS+	18	Device damage.	A
VOUT	19	VOUT = VIN.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

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