Functional Safety Information

UCC27614-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the UCC27614-Q1 (DSG (SON 8), D (SOIC 8), and DGN (VSSOP 8) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagrams for reference.

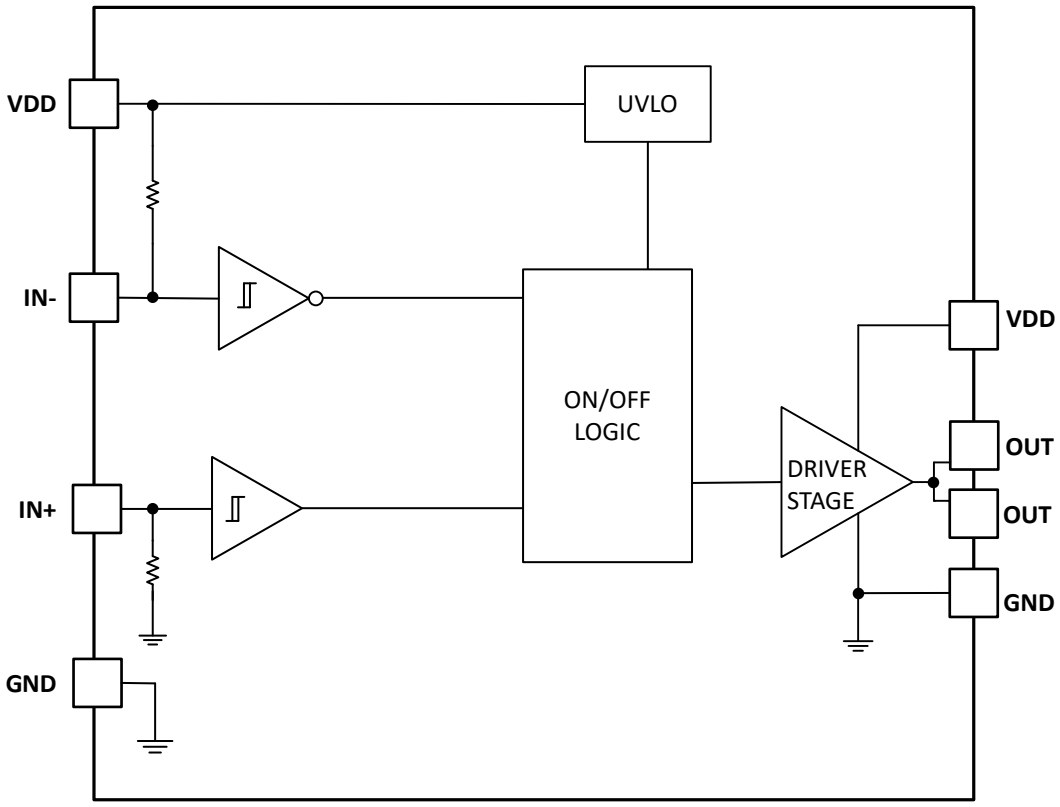

Figure 1-1. Functional Block Diagram (DSG)

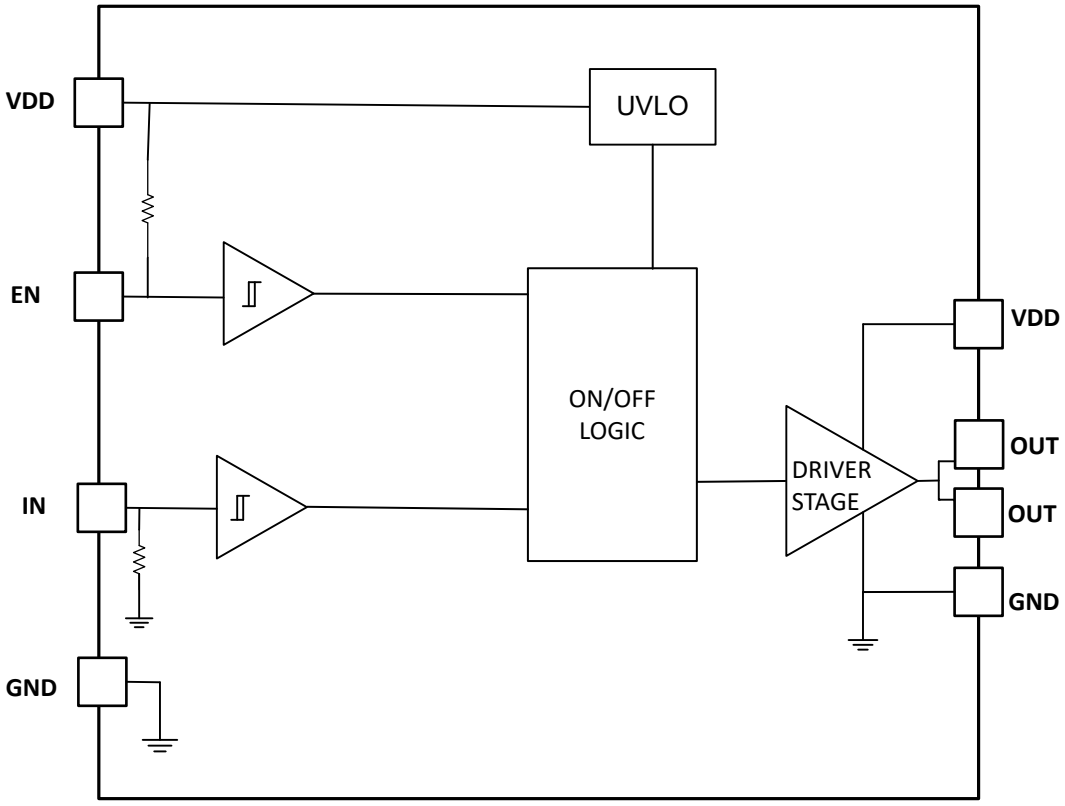

Figure 1-2. Functional Block Diagram (D and DGN)

The UCC27614-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DSG (SON 8) Package

This section provides functional safety failure in time (FIT) rates for the UCC27614-Q1 (DSG (SON 8) package) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	50	5
	350	7
Die FIT rate	50	3
	350	5
Package FIT rate	50	2
	350	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 50mW, 350mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 D (SOIC 8) Package

This section provides functional safety failure in time (FIT) rates for the UCC27614-Q1 (D (SOIC 8) package) based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	50	12
	200	14
Die FIT rate	50	3
	200	5
Package FIT rate	50	9
	200	9

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 50mW, 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 DGN (VSSOP 8) Package

This section provides functional safety failure in time (FIT) rates for the UCC27614-Q1 (DGN (VSSOP 8) package) based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	50	6
	500	9
Die FIT rate	50	3
	500	5
Package FIT rate	50	3
	500	4

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 50mW, 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC27614-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)		
	DSG (SON 8)	D (SOIC 8)	DGN (VSSOP 8)
OUT stuck high	28	14	14
OUT stuck low	28	14	14
OUT functioning out of specification	28	14	14
EN stuck high	N/A	14	14
EN stuck low	N/A	14	14
EN functioning out of specification	N/A	14	14
UVLO false reporting	12	12	12
Test mode | EMI performance	4	4	4

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC27614-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin 1 shorted to pin 8 is not considered.
- Pin 4 shorted to pin 5 is not considered.
- The case of a short-circuit to supply is analyzed as a short to VDD.

4.1 DSG (SON 8) Package

Figure 4-1 shows the UCC27614-Q1 pin diagram for the DSG (SON 8) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC27614-Q1 datasheet.

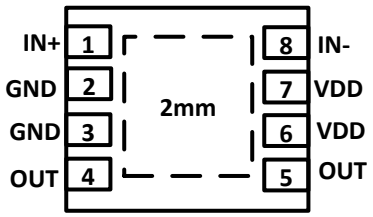

Figure 4-1. Pin Diagram (DSG (SON 8) Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	The function of the IN+ pin is lost. The OUT pin is stuck low.	B
GND	2	There is no impact to the device.	D
GND	3	There is no impact to the device.	D
OUT	4	The OUT pin is stuck low.	A
OUT	5	The OUT pin is stuck low.	A
VDD	6	There is an undervoltage event on the VDD pin. The OUT pin is off.	B
VDD	7	There is an undervoltage event on the VDD pin. The OUT pin is off.	B
IN-	8	The function of the IN- pin is lost. The OUT pin is stuck high.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	The function of the IN+ pin is lost. The OUT pin is stuck low.	B
GND	2	The state of the OUTA and OUTB pins is unknown.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	3	The state of the OUTA and OUTB pins is unknown.	B
OUT	4	The OUT pin is disconnected from the power FET.	B
OUT	5	The OUT pin is disconnected from the power FET.	B
VDD	6	There is an undervoltage event on the VDD pin. The OUT pin is off.	B
VDD	7	There is an undervoltage event on the VDD pin. The OUT pin is off.	B
IN-	8	The function of the IN- pin is lost. The OUT pin is stuck low.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN+	1	GND	The OUT pin is stuck low.	B
GND	2	GND	There is no impact to the device.	D
GND	3	OUT	The OUT pin is stuck low.	B
OUT	5	VDD	The OUT pin is stuck high.	A
VDD	6	VDD	There is no impact to the device.	D
VDD	7	IN-	The OUT pin is stuck low.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	The OUT pin is stuck high.	B
GND	2	The power supply is short circuited.	B
GND	3	The power supply is short circuited.	B
OUT	4	The OUT pin is stuck high.	A
OUT	5	The OUT pin is stuck high.	A
VDD	6	There is no impact to the device.	D
VDD	7	There is no impact to the device.	D
IN-	8	The OUT pin is stuck low.	B

4.2 D (SOIC 8) and DGN (VSSOP 8) Package

Figure 4-2 and Figure 4-3 show the UCC27614-Q1 pin diagrams for the D (SOIC 8) and DGN (VSSOP 8) packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC27614-Q1 datasheet.

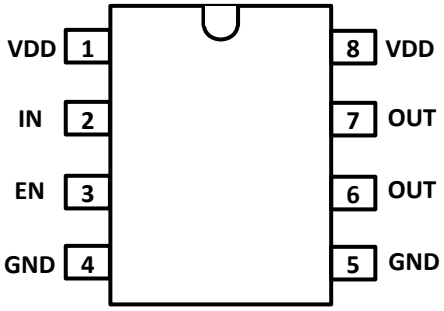

Figure 4-2. Pin Diagram (D (SOIC 8) Package)

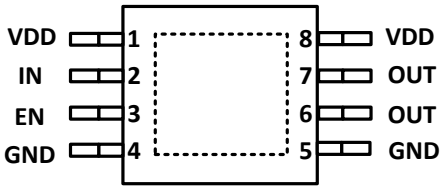

Figure 4-3. Pin Diagram (DGN (VSSOP 8) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	There is an undervoltage event on the VDD pin. The OUT pin is off.	B
IN	2	The function of the IN pin is lost. The OUT pin is stuck low.	B
EN	3	The function of the EN pin is disabled. The OUT pin does not respond to the IN pin.	B
GND	4	There is no impact to the device.	D
GND	5	There is no impact to the device.	D
OUT	6	The OUT pin is stuck low. The OUT pin is shorted if the IN pin is commanded *High*.	A
OUT	7	The OUT pin is stuck low. The OUT pin is shorted if the IN pin is commanded *High*.	A
VDD	8	There is an undervoltage event on the VDD pin. The OUT pin is off.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	There is an undervoltage event on the VDD pin. The OUT pin is off.	B
IN	2	The function of the IN pin is lost. The OUT pin is stuck low.	B
EN	3	The OUT pin is always enabled. The OUT pin responds to the IN pin.	B
GND	4	The state of the OUT pin is unknown.	B
GND	5	The state of the OUT pin is unknown.	B
OUT	6	The OUT pin is disconnected from the power FET.	B
OUT	7	The OUT pin is disconnected from the power FET.	B
VDD	8	There is an undervoltage event on the VDD pin. The OUT pin is off.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDD	1	IN	The OUT pin is stuck high.	B
IN	2	EN	The EN pin cannot override the command of the IN pin. The OUT pin responds to the IN pin.	B
EN	3	GND	The function of the EN pin is disabled. The OUT pin does not respond to the IN pin.	B
GND	5	OUT	The OUT pin is stuck low. The OUT pin is short circuited if the IN pin is commanded *High*.	A
OUT	6	OUT	There is no impact to the device.	D
OUT	7	VDD	The OUT pin is stuck high.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	There is no impact to the device.	D
IN	2	The OUT pin is stuck high.	B
EN	3	The OUT pin is always enabled. The OUT pin responds to the IN pin.	B
GND	4	The power supply is short circuited.	B
GND	5	The power supply is short circuited.	B
OUT	6	The OUT pin is stuck high.	A
OUT	7	The OUT pin is stuck high.	A
VDD	8	There is no impact to the device.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

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