Functional Safety Information

TCAN1043N-Q1 and TCAN1473-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

Table of Contents

List of Figures

List of Tables

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1 Overview

This document contains information for the TCAN1043N-Q1 and TCAN1473-Q1 to aid in a functional safety system design. This is a controller area network (CAN) transceiver in the SOIC (D), VSON (DMT), and SOT (DYY) packages to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (FMA) for the device pins of TCAN1043N-Q1 and TCAN1473-Q1

Figure 1-1 shows the device functional block diagram for reference.

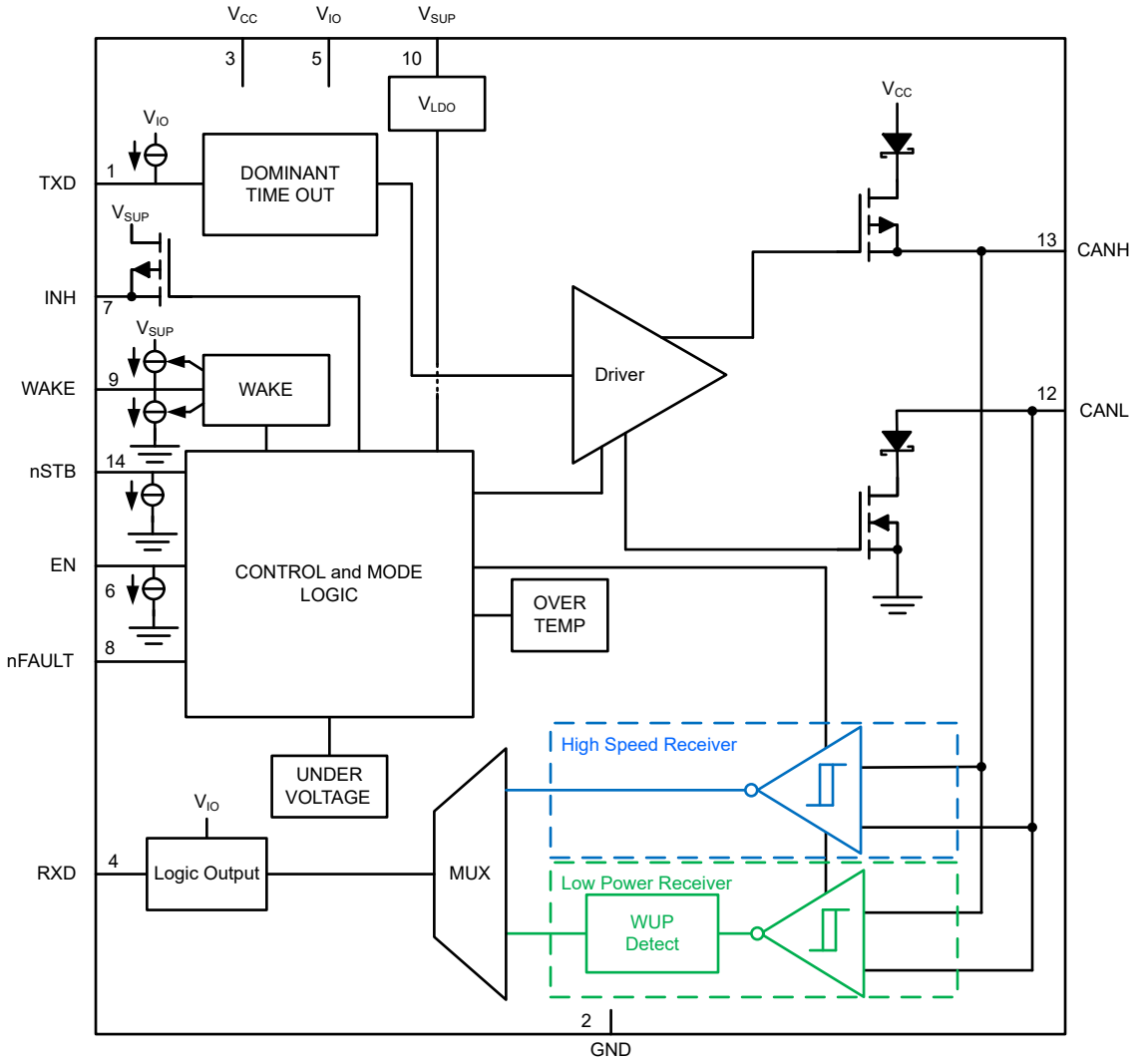

Figure 1-1. TCAN1043N-Q1 and TCAN1473-Q1 Functional Block Diagram

TCAN1043N-Q1 and TCAN1473-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TCAN1043N-Q1 and TCAN1473-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 14-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 14-pin VSON (DMT)	FIT (Failures Per 10^9 Hours) 14-pin SOT (DYY)
Total component FIT rate	22	10	11
Die FIT rate	6	4	7
Package FIT rate	16	6	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 353mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs analog and mixed ≤ 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN1043N-Q1 and TCAN1473-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Receiver fail	35
Transmitter fail	35
System stuck in sleep mode	15
Control and mode logic failure	10
CANL or CANH driver stuck dominant	5

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TCAN1043N-Q1 and TCAN1473-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{CC} (see Table 4-5)
- Pin short-circuited to V_{SUP} (see Table 4-6)
- Pin short-circuited to V_{IO} (Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the SOIC (D) pin diagram. Figure 4-2 shows the VSON (DMT) pin diagram. Figure 4-3 shows the SOT (DYY) pin diagram.

For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN1043N-Q1 and TCAN1473-Q1 data sheets.

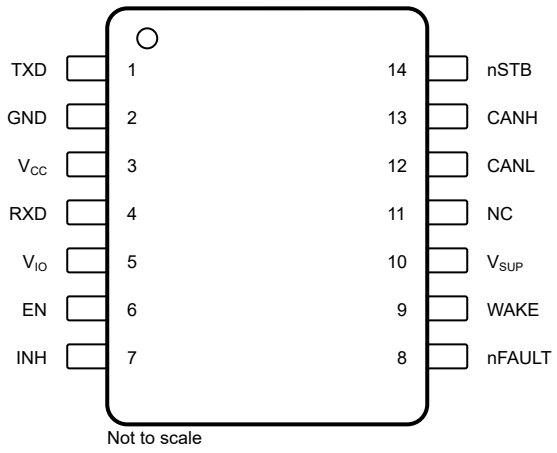

Figure 4-1. SOIC (D) Pin Diagram

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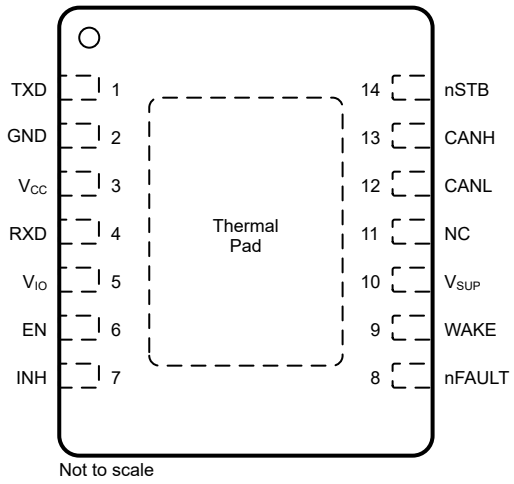

Figure 4-2. VSON (DMT) Pin Diagram

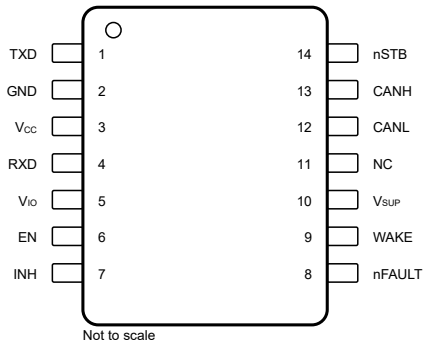

Figure 4-3. SOT (DYY) Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- V_{CC} = 4.5V to 5.5V
- V_{SUP} = 4.5V to 40V
- V_{IO} = 1.7V to 5.5V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD biased dominant indefinitely. The device enters dominant time-out mode. Unable to transmit data.	B
GND	2	None.	D
V_{CC}	3	Device enters Sleep mode. There is a high current draw from the external regulator that supplies to the VCC pin.	B
RXD	4	Receiver output biased recessive indefinitely. The host is unable to receive data from the bus.	B
V_{IO}	5	Device enters Sleep mode. Transceiver is passive on bus. There is a high current draw from the external regulator that supplies to VIO.	B
EN	6	EN pin biased low. The device is not able to enter normal mode. Unable to communicate.	B
INH	7	High I_{SUP} current, the INH pin can be damaged and indication from sleep mode transition is not available.	A
nFAULT	8	nFAULT pin biased low indefinitely, which indicates a fault indefinitely.	B
WAKE	9	WAKE pin biased low indefinitely and is not able to utilize the local wake-up function.	B
V_{SUP}	10	Device is not powered. There will be a high current flowing from the source supplying to the V_{SUP} pin (battery) to the ground.	B
NC	11	None.	D
CANL	12	$V_{O(REC)}$ specification is violated, degraded EMC performance.	C
CANH	13	Device cannot drive dominant bit to the bus, no communication possible.	B
nSTB	14	nSTB biased low indefinitely. The transceiver is unable to enter normal mode. Unable to communicate.	B
Thermal Pad	-	None.	D

Note

The VSON package includes a thermal pad.

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD pin defaults to a recessive bias. The device is always recessive and unable to transmit data.	B
GND	2	Device is not powered.	B
V_{CC}	3	Device is in protected mode.	B
RXD	4	No RXD output, unable to receive data.	B
V_{IO}	5	Device is in protected mode.	B
EN	6	EN pin defaults to a logic-low bias. The device is not able to enter normal mode. Unable to communicate.	B
INH	7	None.	D
nFAULT	8	No effect on the device performance, unable to monitor system faults.	B
WAKE	9	No effect on the device performance, unable to use the local wake-up function.	B
V_{SUP}	10	Device is not powered.	B
NC	11	None.	D
CANL	12	Device cannot drive dominant on bus and is unable to communicate.	B
CANH	13	Device cannot drive dominant on bus and is unable to communicate.	B
nSTB	14	nSTB defaults to a logic-low bias. The device is not able to enter normal mode. Unable to communicate.	B
Thermal Pad	-	None.	D

Note

The VSON package includes a thermal pad.

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
TXD	1	GND	TXD is biased dominant indefinitely. The device enters dominant time-out mode. Unable to transmit data.	B
GND	2	VCC	Device is in protected mode, high I_{CC} current.	B
V_{CC}	3	RXD	RXD output biased recessive indefinitely. The controller is unable to receive data from CAN bus.	B
RXD	4	VIO	RXD output biased recessive indefinitely. The controller is unable to receive data from CAN bus.	B
VIO	5	EN	EN pin biased high indefinitely. The device is unable to enter standby and silent mode.	B
EN	6	INH	Absolute maximum violation on the EN pin, except in sleep mode. Transceiver can be damaged.	A
nFAULT	8	WAKE	Potential absolute maximum violation on nFAULT pin if WAKE is biased high. Transceiver can be damaged.	A
WAKE	9	VSUP	WAKE biased high indefinitely, unable to utilize the local wake-up function.	B
V_{SUP}	10	NC	None.	D
NC	11	CANL	None.	D
CANL	12	CANH	Bus biased recessive. No communication is possible. I_{OS} current can be reached on CANH/CANL.	B
CANH	13	nSTB	Driver and receiver turn off when the CAN bus is recessive. Potentially does not enter normal mode.	B

Note

The VSON package includes a thermal pad. All device pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad.

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Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD biased recessive indefinitely, unable to transmit data.	B
GND	2	CAN transmitter is not powered and the device enters Sleep mode. There is a high current draw from the external regulator supplying to the VCC pin.	B
V_{CC}	3	None.	D
RXD	4	Receiver output biased recessive indefinitely. Host is unable to receive data from bus.	B
V_{IO}	5	I/O pins operate as 5V inputs and outputs. Microcontroller can be damaged if VCC > VIO.	C
EN	6	EN biased high indefinitely. The device is unable to enter standby and silent mode.	B
INH	7	Absolute maximum violation on VCC pin. INH is biased at VCC voltage. System potentially does not wake up.	A
nFAULT	8	nFAULT biased high indefinitely. The transceiver is unable to report faults.	B
WAKE	9	None.	D
V_{SUP}	10	Absolute maximum violation on VCC.	A
NC	11	None.	D
CANL	12	I_{OS} current can be reached, RXD is always recessive.	B
CANH	13	$V_{O(REC)}$ specification is violated, degraded EMC performance.	C
nSTB	14	nSTB biased high indefinitely. The transceiver is unable to enter standby and sleep mode.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to V_{SUP}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	Absolute maximum violation, transceiver can be damaged.	A
GND	2	Device is not powered, high I_{SUP} current.	B
V_{CC}	3	Absolute maximum violation, transceiver can be damaged.	A
RXD	4	Absolute maximum violation, transceiver can be damaged.	A
V_{IO}	5	Absolute maximum violation, transceiver can be damaged.	A
EN	6	Absolute maximum violation, transceiver can be damaged.	A
INH	7	Minimal current driven into the INH pin.	D
nFAULT	8	Absolute maximum violation, transceiver can be damaged.	A
WAKE	9	WAKE biased high, unable to use the local wake-up function.	B
V_{SUP}	10	None.	D
NC	11	None.	D
CANL	12	I_{OS} current can be reached. RXD is always recessive.	B
CANH	13	$V_{O(REC)}$ specification is violated, degraded EMC performance and communication errors can also result.	C
nSTB	14	Absolute maximum violation, transceiver can be damaged.	A

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Table 4-7. Pin FMA for Device Pins Short-Circuited to V_{IO}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD biased recessive indefinitely, unable to transmit data.	B
GND	2	Device is not powered. There is a high current draw from the external regulator supplying to the VIO pin.	B
V_{CC}	3	I/O pins operate as 5V inputs and outputs. Microcontroller can be damaged if VCC > VIO.	C
RXD	4	Receiver output biased recessive indefinitely. Host is unable to receive data from bus.	B
V_{IO}	5	None.	D
EN	6	EN biased high indefinitely. The device is unable to enter standby and silent mode.	B
INH	7	Absolute maximum violation on the VIO pin. INH is biased at VIO voltage. System potentially does not wake up.	A
nFAULT	8	nFAULT biased high indefinitely. The transceiver is unable to report faults.	B
WAKE	9	None.	D
V_{SUP}	10	Absolute maximum violation on VIO.	A
NC	11	None.	D
CANL	12	I_{OS} current can be reached, RXD is always recessive.	B
CANH	13	$V_{O(REC)}$ specification is violated, degraded EMC performance.	C
nSTB	14	nSTB biased high indefinitely. The transceiver is unable to enter standby and sleep mode.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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