Functional Safety Information

SN74AVC4T774-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for SN74AVC4T774-Q1 (TSSOP, VQFN, and UQFN packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device

Figure 1-1 shows the device functional block diagram for reference.

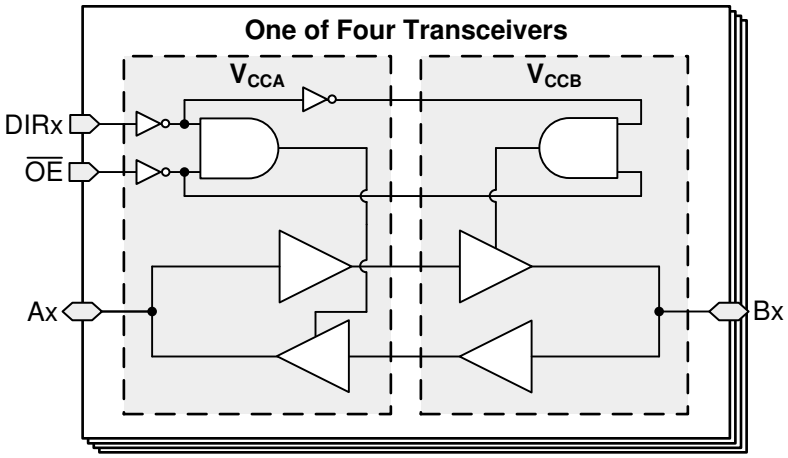

Figure 1-1. Functional Block Diagram

SN74AVC4T774-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 TSSOP Package

This section provides Functional Safety Failure In Time (FIT) rates for TSSOP package of SN74AVC4T774-Q1:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	15
Die FIT Rate	2
Package FIT Rate	13

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 19 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Bus interface LVT, ALVT	5 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VQFN Package

This section provides Functional Safety Failure In Time (FIT) rates for the VQFN package of SN74AVC4T774-Q1:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	2
Package FIT Rate	5

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 19 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Bus interface LVT, ALVT	5 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 UQFN Package

This section provides Functional Safety Failure In Time (FIT) rates for the UQFN package of SN74AVC4T774-Q1:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	8
Die FIT Rate	2
Package FIT Rate	6

The failure rate and mission profile information in Table 2-5 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 19 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Bus interface LVT, ALVT	5 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74AVC4T774-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Driver HIZ no output	18%
Output functional – out of specification timing or voltage	27%
Driver stuck at fault high	21%
Driver stuck at fault low	24%
Driver stuck at undetermined state	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74AVC4T774-Q1 (TSSOP and VQFN packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 and Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1, Figure 4-2, and Figure 4-3 show the SN74AVC4T774-Q1 pin diagrams for the TSSOP, VQFN, and UQFN packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74AVC4T774-Q1 data sheet.

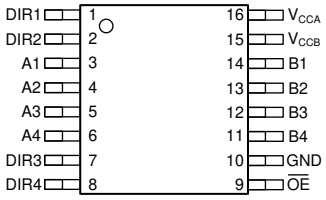

Figure 4-1. Pin Diagram (TSSOP) Package

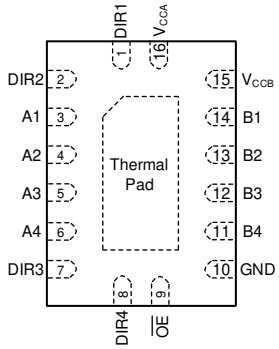

Figure 4-2. Pin Diagram (VQFN Package)

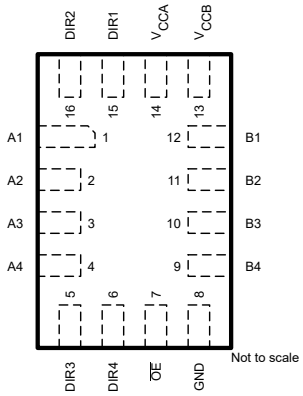

Figure 4-3. Pin Diagram (UQFN Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DIR1	1	Direction control will fix B --> A direction	B
DIR2	2		
A1	3	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
A2	4		
A3	5		
A4	6		
DIR3	7	Direction control will fix B --> A direction	B
DIR4	8		
$\overline{OE}$	9	All outputs will be active, device cannot be disabled	B
GND	10	Normal operation	D
B4	11	If configured as an output then damage is possible. If configured as an input, no damage occurs, but output will not switch	A
B3	12		
B2	13		
B1	14		
VCCB	15	GND short to VCC, device will be bypassed; may cause system damage, but no damage to the device.	B
VCCA	16		

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	16	GND short to VCC, device will be bypassed; can cause system damage, but not device damage	B
GND	10	Device will not be powered	B
A	3-6	If configured as output, normal operation. If configured as input, pin is floating which could cause excessive current	A
B	11-14	If configured as output, normal operation. If configured as input, pin is floating which could cause excessive current.	A
DIR	1-2 7-8	Pin is floating which can cause excessive current	A
VCCB	15	GND short to VCC, device will be bypassed; can cause system damage, but no damage to the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
DIR1	1	DIR2	If both HIGH, direction control will fix A --> B direction. If both LOW, direction control will fix B --> A direction. If one DIR is HIGH and the other is LOW, bus contention during transitions can occur and may cause high current	A
DIR2	2	A1	If DIR2 is LOW, A2 will be an output and damage is possible. If DIR3 is HIGH, A2 will be an input and drive the output B2 LOW	A
A1	3	A2	If A(n) and A(n+1) are configured as outputs then damage is possible. If configured as inputs, both bits will always have the same value	A
A2	4	A3		
A3	5	A4		
A4	6	DIR3	If DIR3 is LOW, A3 will be an output and damage is possible. If DIR3 is HIGH, A3 will be an input and drive the output B3 LOW	A
DIR3	7	DIR4	If both HIGH, direction control will fix A --> B direction. If both LOW, direction control will fix B --> A direction. If one DIR is HIGH and the other is LOW, bus contention during transitions could occur and may cause high current	A
DIR4	8	$\overline{OE}$	If $\overline{OE}$ is HIGH, I/Os will be placed in Hi-Z. If both DIR and $\overline{OE}$ are LOW, direction control will fix B --> A direction. If DIR is HIGH and the $\overline{OE}$ is LOW, direction control will fix A --> B direction.	B
$\overline{OE}$	9	GND	All outputs will be active; device cannot be disabled	B
GND	10	B4	If B4 is configured as an output then damage is possible. If configured as input, output A4 will be fixed LOW	A
B4	11	B3	If B(n) and B(n+1) are configured as outputs then damage is possible. If configured as inputs, both bits will always have the same value.	A
B3	12	B2		
B2	13	B1		
B1	14	VCCB	If B1 is configured as an output then damage is possible. If configured as input, no damage, but output A1 will remain high.	A
VCCB	15	VCCA	GND short to VCC, device will be bypassed; may cause system damage, but not device damage	B
VCCA	16	DIR1	Direction control will fix A --> B direction	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCCA

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	16	Normal operation	D
GND	10	GND short to VCC, device will be bypassed; may cause system damage, but not device damage	B
A	3-6	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
B	11-14	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL is not met	A
DIR	1-2, 7-8	Direction control will fix A --> B direction	B
$\overline{OE}$	9	I/Os will be placed in Hi-Z	B
VCCB	15	VCCA short to VCCB, device will be bypassed; may cause system damage, but not device damage	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to VCCB

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	16	VCCA short to VCCB, device will be bypassed; can cause system damage, but not device damage	B
GND	10	GND short to VCC, device will be bypassed; can cause system damage, but not device damage	B
A	3-6	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL is not met	A
B	11-14	If configured as an output, then damage is possible. If configured as an input, no damage occurs, but output will not switch.	A
DIR	1-2, 7-8	If VCCB>VCCA, DIR will fix B --> A direction OR if VCCB < VCCA, input can be at an inappropriate logic level, which can cause damage	B
$\overline{OE}$	9	I/Os will be placed in Hi-Z	B
VCCB	15	Normal operation	D

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