Functional Safety Information

SN74AVC2T45-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for SN74AVC2T45-Q1 (DCU package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

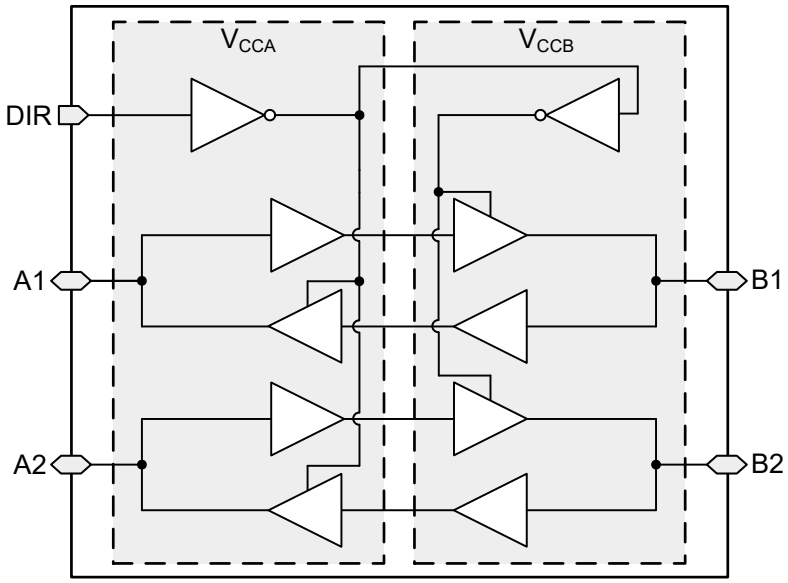

Figure 1-1. Functional Block Diagram

SN74AVC2T45-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for SN74AVC2T45-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 10 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS Logic	12 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74AVC2T45-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Driver HIZ; no output	28%
Output functional – out of specification timing or voltage	27%
Driver stuck at fault high	18%
Driver stuck at fault low	18%
Driver stuck at undetermined state	9%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN74AVC2T45-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VCCA (see Table 4-5)
- Pin short-circuited to VCCB (see Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the SN74AVC2T45-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the SN74AVC2T45-Q1 data sheet.

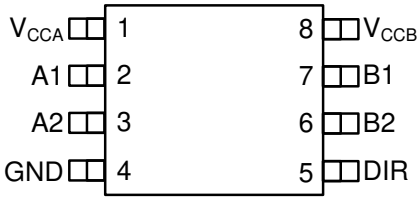

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VCCA (see Table 4-5)
- Pin short-circuited to VCCB (see Table 4-6)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	GND short to VCC, device will be bypassed; may cause system damage, but damage to the device does not occur	B
A1	2	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
A2	3	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
GND	4	Normal operation	D
DIR	5	Direction control will fix B --> A direction	B
B2	6	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
B1	7	If configured as an output then damage is possible. If configured as input, no damage occurs, but output will not switch	A
VCCB	8	GND short to VCC, device will be bypassed; may cause system damage, but damage to the device does not occur	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Device will not be powered	B
A1	2	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
A2	3	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
GND	4	Device will not be powered	B
DIR	5	Pin is floating which could cause excessive current	A
B2	6	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
B1	7	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
VCCB	8	Device will not be powered	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	A1	If configured as an output then damage is possible. If configured as input, no damage occurs, but output will not switch	A
A1	2	A2	Two inputs shorted together will not cause damage unless there is external bus contention that drives the input such that VIL < Input Voltage < VIH in which case excessive supply current to GND may cause damage. Two outputs shorted together may cause damage if there is external bus contention that drives one output LOW while driving the other output HIGH. If both outputs are HIGH or both outputs are LOW, then nothing will occur; no damage.	A
A2	3	GND	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
GND	4	DIR	Direction control will fix B --> A direction	B
DIR	5	B2	If DIR is LOW, B will be an input and drive the output low. If DIR is HIGH, B will be an output and damage is possible based on state of A	A
B2	6	B1	Two inputs shorted together will not cause damage unless there is external bus contention that drives the input such that VIL is less than Input Voltage is less than VIH in which case excessive supply current to GND may cause damage. Two outputs shorted together may cause damage if there is external bus contention that drives one output LOW while driving the other output HIGH. If both outputs are HIGH or both outputs are LOW, then nothing will occur, no damage occurs.	A
B1	7	VCCB	If configured as an output then damage is possible. If configured as input, no damage occurs, but output will not switch	A
VCCB	8	VCCA	VCCB short to VCCA, device will be bypassed; may cause system damage, but no damage to the device occurs	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCCA

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Normal operation	D
A1	2	If configured as an output then damage is possible. If configured as input, no damage occurs, but output will not switch	A
A2	3	If configured as an output then damage is possible. If configured as input, no damage occurs, but output will not switch	A
GND	4	GND short to VCC, device will be bypassed; may cause system damage, but no damage to the device occurs	B
DIR	5	Direction control will fix A --> B direction	B
B2	6	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL is not met	A
B1	7	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL is not met	A
VCCB	8	VCCA short to VCCB, device will be bypassed; may cause system damage, but no damage to the device occurs	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to VCCB

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	VCCB short to VCCA, device will be bypassed - may cause system damage, but damage to the device does not occur	B
A1	2	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL is not met	A
A2	3	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL is not met	A
GND	4	GND short to VCC, device will be bypassed; may cause system damage, but damage to the device does not occur	B
DIR	5	If VCCB>VCCA, DIR will fix B --> A direction OR if VCCB<VCCA, input could be inappropriate logic level potentially causing damage	A
B2	6	If configured as an output then damage is possible. If configured as input, damage does not occur, but output will not switch	A
B1	7	If configured as an output then damage is possible. If configured as input, damage does not occur, but output will not switch	A
VCCB	8	Normal operation	D

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