Functional Safety Information

LMR604x0, LMR604x0-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1 (RAK package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

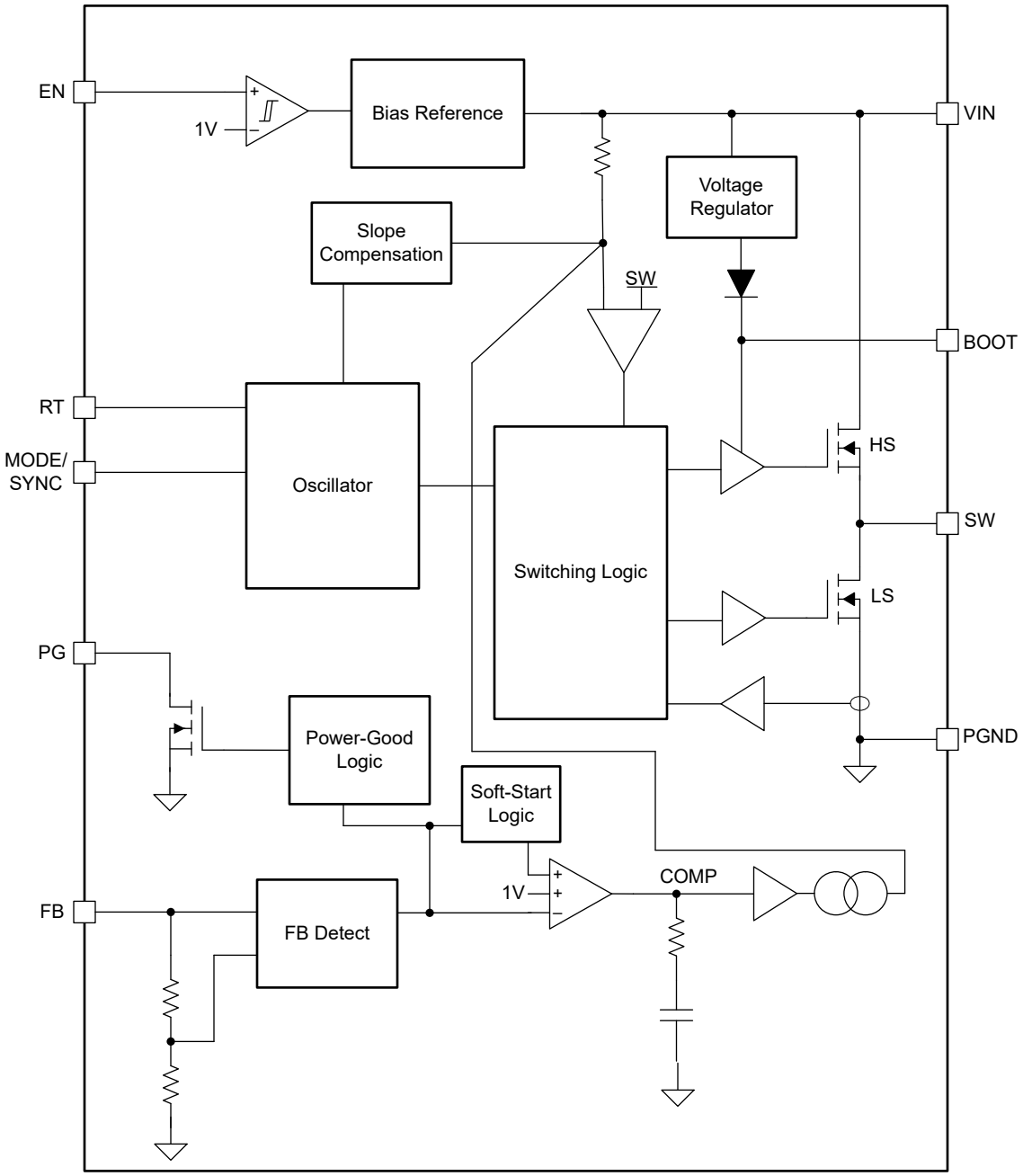

Figure 1-1. Functional Block Diagram

The LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	5
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 640mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs analog and mixed ≤50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60
Output voltage not in specification - voltage or timing	30
Gate driver stuck on	5
Power good false trip or failure to trip	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1 data sheet.

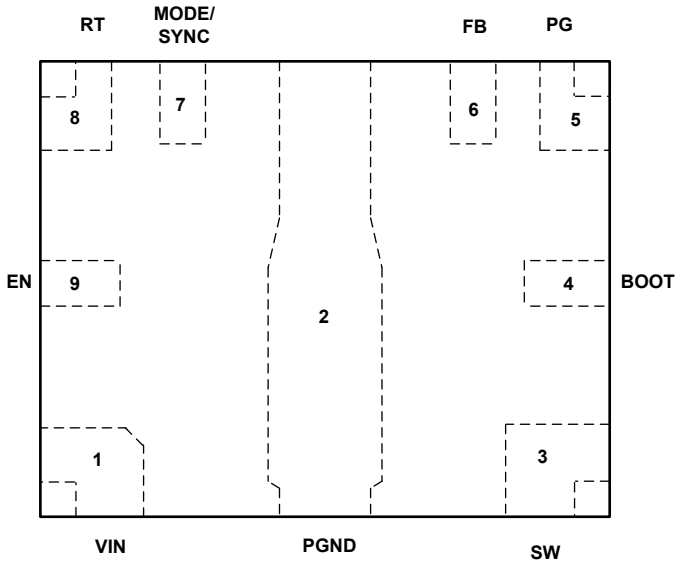

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The application circuit is used according to the LMR60430, LMR60430-Q1, LMR60440, and LMR60440-Q1 data sheets.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	V_{OUT} = 0V.	B
PGND	2	V_{OUT} is normal.	D
SW	3	Damage to high-side FET.	A
BOOT	4	V_{OUT} = 0V. High-side FET does not turn on.	B
PG	5	When not in use, this pin can be left grounded (PG is not a valid signal and VOUT is normal).	D
FB	6	When in adjustable output mode, V_{OUT} approaches VIN. When in fixed output mode, V_{OUT} = 0V.	B
MODE/SYNC	7	Device switches in AUTO mode. V_{OUT} is normal.	D
RT	8	Device stops switching until short to GND is removed.	B
EN	9	V_{OUT} = 0V. Enable is below the V_{EN-TH} and functionality is halted.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	V_{OUT} = 0V.	B
PGND	2	V_{OUT} can be abnormal.	C
SW	3	V_{OUT} = 0V.	B
BOOT	4	V_{OUT} = 0V. High-side FET does not turn on.	B
PG	5	When not in use, this pin can be left open (PGOOD is not a valid signal and V_{OUT} is normal).	D
FB	6	V_{OUT} approaches VIN.	C
MODE/SYNC	7	Mode of operation can toggle between AUTO and FPWM.	C
RT	8	Internal clock does not operate properly and the part does not switch.	B
EN	9	Pin cannot be left floating. Device potentially does not enable.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VIN	1	PGND	V_{OUT} = 0V.	B
PGND	2	SW	Damage to high-side FET.	A
SW	3	BOOT	V_{OUT} = 0V, high-side FET does not turn on and there is not C_{BOOT}.	B
BOOT	4	PG	PG damage occurs if BOOT voltage is greater than PG absolute maximum voltage.	B
PG	5	FB	In fixed output mode, V_{OUT} = 0V. In adjustable mode, if a short happens before soft state is complete, output voltage approaches input voltage supply.	B
FB	6	PGND	In fixed output mode, V_{OUT} = 0V. In adjustable output mode, output voltage approaches the input voltage supply.	B
MODE/SYNC	7	RT	Device operates in FPWM.	D
RT	8	EN	Internal clock does not switch at the correct frequency.	C
EN	9	VIN	Device is enabled once the voltage between VIN and PGND is greater than $VIN_{UVLO(R)}$.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	V_{OUT} is normal.	D
PGND	2	V_{OUT} = 0V.	B
SW	3	Damage to low-side FET.	A
BOOT	4	Damage occurs to BOOT ESD.	A
PG	5	If supply voltage is greater than 20V, damage occurs to PGOOD pin.	A
FB	6	If supply voltage is greater than 16V, damage occurs.	A
MODE/SYNC	7	Device operates in FPWM.	D
RT	8	Internal clock does not switch at the correct frequency.	C
EN	9	V_{OUT} is normal.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

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