Functional Safety Information

AFE539F1-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the AFE539F1-Q1 (RTE package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

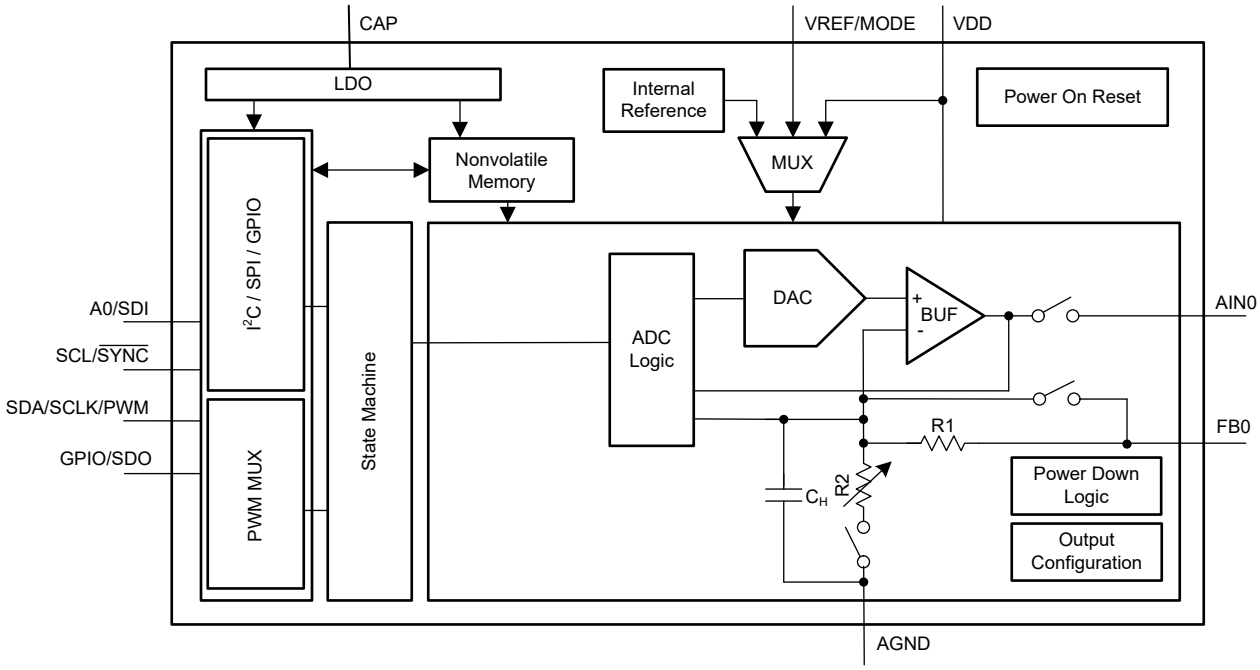

Figure 1-1. Functional Block Diagram

The AFE539F1-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the AFE539F1-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	2
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 50 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the AFE539F1-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Digital core, state machine, and interface failure	51
NVM (EEPROM/OTP) retention loss	17
Reference failure	5
POR failure	5
ADC failure	22

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the AFE539F1-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the AFE539F1-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the AFE539F1-Q1 data sheet.

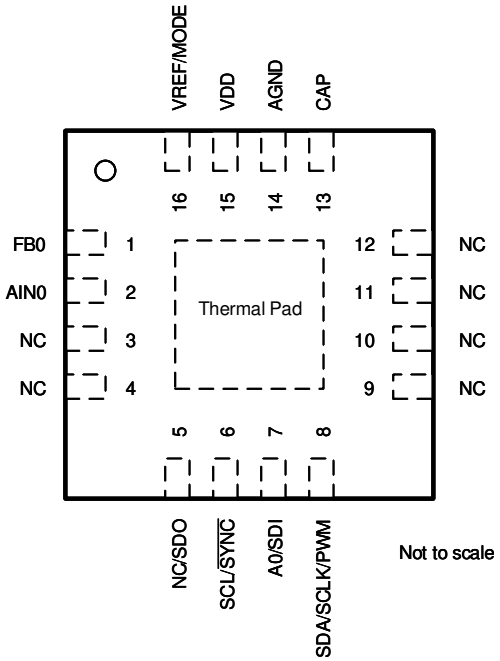

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All the pin FMA analysis are described based on Figure 1-1.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB0	1	ADC and PWM duty cycle performance degradation	C
AIN0	2	Loss of ADC functionality and PWM output duty cycle is stuck to maximum duty cycle	B
NC	3	No change in functionality or performance	D
NC	4	No change in functionality or performance	D
NC/SDO	5	Loss of SDO functionality and read back data is not available	B
SCL/$\overline{\text{SYNC}}$	6	Loss of communication with the device	B
A0/SDI	7	Loss of communication with the device	B
SDA/SCLK/PWM	8	Loss of communication and PWM functionality with the device	B
NC	9	No change in functionality or performance	D
NC	10	No change in functionality or performance	D
NC	11	No change in functionality or performance	D
NC	12	No change in functionality or performance	D
CAP	13	Loss of functionality, device enters short circuit protection, power consumption increases	B
AGND	14	No change in functionality or performance	D
VDD	15	Complete loss of functionality, no device damage	B
VREF/MODE	16	Loss of core DAC functionality and PWM mode	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB0	1	ADC and PWM duty cycle performance degradation	C
AIN0	2	ADC input is not available and PWM output duty cycle will be corrupted	B
NC	3	No change in functionality or performance	D
NC	4	No change in functionality or performance	D
NC/SDO	5	Loss of SDO functionality and read back data is not available	B
SCL/$\overline{\text{SYNC}}$	6	Loss of communication with the device	B
A0/SDI	7	Loss of communication with the device	B
SDA/SCLK/PWM	8	Loss of communication and PWM functionality is not available	B
NC	9	No change in functionality or performance	D
NC	10	No change in functionality or performance	D
NC	11	No change in functionality or performance	D
NC	12	No change in functionality or performance	D
CAP	13	Open-circuited pin can cause damage to the low-voltage digital core and NVM supplied by the internal LDO	A
AGND	14	Complete loss of functionality, no device damage	B
VDD	15	Complete loss of functionality, no device damage	B
VREF/MODE	16	Loss of core DAC functionality and PWM mode	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FB0	1	VREF/MODE	Short to corner pin is not expected	D
		AIN0	ADC and PWM duty cycle performance degradation	C
AIN0	2	FB0	ADC and PWM duty cycle performance degradation	C
		NC	No change in functionality or performance	D
NC	3	AIN0	No change in functionality or performance	D
		NC	No change in functionality or performance	D
NC	4	NC	No change in functionality or performance	D
		NC/SDO	Short to corner pin is not expected	D
NC/SDO	5	NC	Short to corner pin is not expected	D
		SCL/$\overline{\text{SYNC}}$	Loss of communication with the device, SDO functionality and read back data is not available	B
SCL/$\overline{\text{SYNC}}$	6	NC/SDO	Loss of communication with the device, SDO functionality and read back data is not available	B
		A0/SDI	Loss of communication with the device	B
A0/SDI	7	SCL/$\overline{\text{SYNC}}$	Loss of communication with the device	B
		SDA/SCLK/PWM	Loss of communication and PWM functionality with the device	B
SDA/SCLK/PWM	8	A0/SDI	Loss of communication and PWM functionality with the device	B
		NC	Short to corner pin is not expected	D
NC	9	SDA/SCLK/PWM	Short to corner pin is not expected	D
		NC	No change in functionality or performance	D
NC	10	NC	No change in functionality or performance	D
		NC	No change in functionality or performance	D
NC	11	NC	No change in functionality or performance	D
		NC	No change in functionality or performance	D
NC	12	NC	No change in functionality or performance	D
		CAP	Short to corner pin is not expected	D
CAP	13	NC	Short to corner pin is not expected	D
		AGND	Device enters short circuit protection, power consumption increases	B
AGND	14	CAP	Device enters short circuit protection, power consumption increases	B
		VDD	Complete loss of functionality, no device damage	B
VDD	15	AGND	Complete loss of functionality, no device damage	B
		VREF/MODE	Loss of partial functionality that includes I2C/SPI communication with device, external reference mode and internal reference mode	B
VREF/MODE	16	VDD	Loss of partial functionality that includes I2C/SPI communication with device, external reference mode and internal reference mode	B
		FB0	Short to corner pin is not expected	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB0	1	ADC and PWM duty cycle performance degradation	C
AIN0	2	Loss of ADC functionality and PWM output duty cycle is stuck to minimum duty cycle	B
NC	3	No change in functionality or performance	D
NC	4	No change in functionality or performance	D
NC/SDO	5	Loss of SDO functionality and read back data will be corrupted	B
SCL/SYNC	6	Loss of communication with the device	B
A0/SDI	7	Loss of communication with the device	B
SDA/SCLK/PWM	8	Loss of communication and PWM functionality with the device	B
NC	9	No change in functionality or performance	D
NC	10	No change in functionality or performance	D
NC	11	No change in functionality or performance	D
NC	12	No change in functionality or performance	D
CAP	13	Shorting to VDD pin can cause damage to the low-voltage digital core and NVM supplied by the internal LDO	A
AGND	14	Complete loss of functionality, no device damage	B
VDD	15	No change in functionality or performance	D
VERF/MODE	16	Loss of partial functionality that includes I2C/SPI communication with device, external reference mode and internal reference mode	B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265