Functional Safety Information

DACx3204-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the DACx3204-Q1 (RTE package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

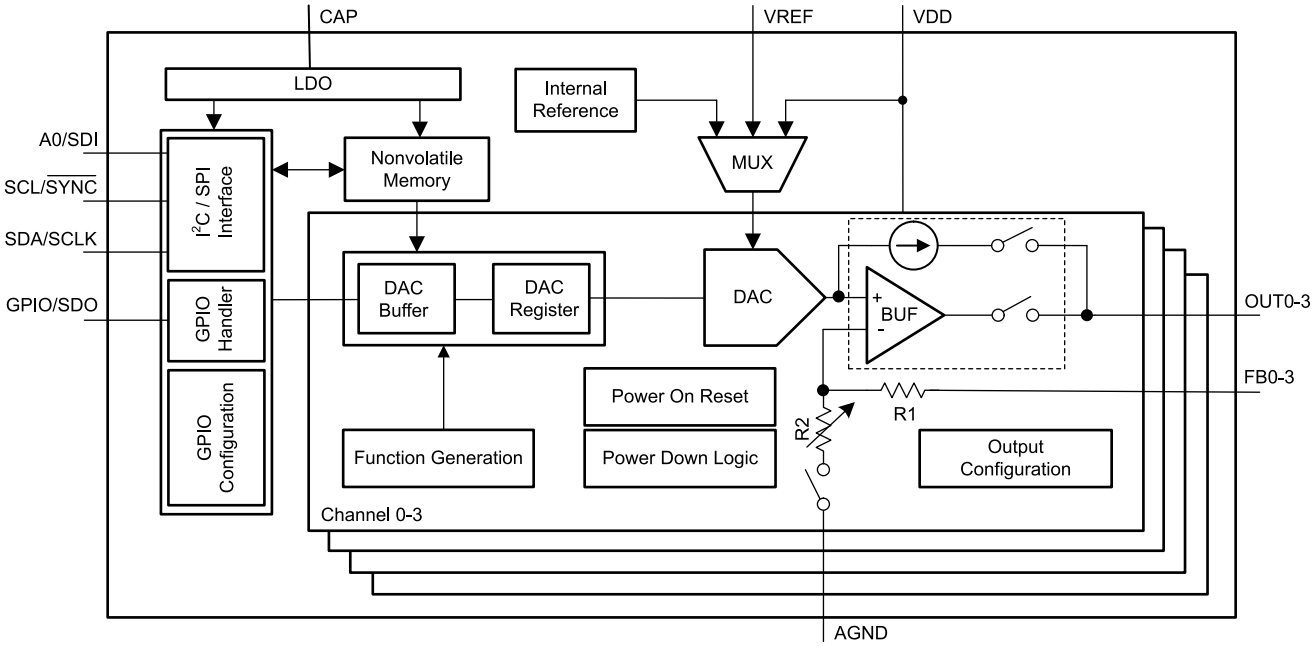

Figure 1-1. Functional Block Diagram

The DACx3204-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the DACx3204-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	2
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 50 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the DACx3204-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or over stress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Digital core and interface failure	29
NVM retention loss	10
POR failure	5
Reference failure	5
DAC output failure	51

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the DACx3204-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuit to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the DACx3204-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DACx3204-Q1 data sheet.

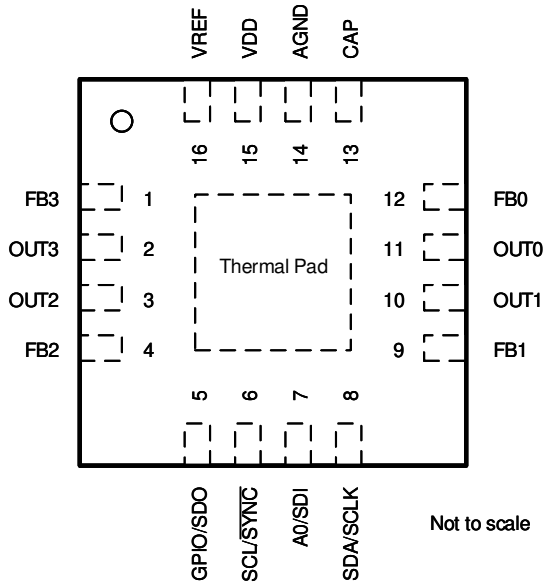

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All the pin FMA analysis data is described based on the Figure 1-1.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB3	1	Voltage output mode; OUT3 voltage value is always high	B
		Current output mode; no change in functionality or performance of OUT3	D
OUT3	2	Voltage output mode; OUT3 will always be stuck at zero in case OUT3 is configured as open drain pull down	B
		Voltage output mode; device can sustain damage over a period of time in case of OUT3 is configured in push-pull mode	A
		Current output mode; output compliance voltage violation and loss of performance	C
OUT2	3	Voltage output mode; OUT2 will always be stuck at zero in case OUT2 is configured as open drain pull down	B
		Voltage output mode; device can sustain damage over a period of time in case of OUT2 is configured in push-pull mode	A
		Current output mode; output compliance voltage violation and loss of performance	C
FB2	4	Voltage output mode; OUT2 voltage value is always high	B
		Current output mode; no change in functionality or performance of OUT2	D
GPIO/SDO	5	Loss of GPIO functionality and read back data will be corrupted	B
SCL/$\overline{\text{SYNC}}$	6	Loss of communication with the device	B
A0/SDI	7	Loss of communication with the device	B
SDA/SCLK	8	Loss of communication with the device	B
FB1	9	Voltage output mode; OUT1 voltage value is always high	B
		Current output mode; no change in functionality or performance of OUT1	D
OUT1	10	Voltage output mode; OUT1 will always be stuck at zero in case OUT1 is configured as open drain pull down	B
		Voltage output mode; device can sustain damage over a period of time in case of OUT1 is configured in push-pull mode	A
		Current output mode; output compliance voltage violation and loss of performance	C
OUT0	11	Voltage output mode; OUT0 will always be stuck at zero in case OUT0 is configured as open drain pull down	B
		Voltage output mode; device can sustain damage over a period of time in case of OUT0 is configured in push-pull mode	A
		Current output mode; output compliance voltage violation and loss of performance	C
FB0	12	Voltage output mode; OUT0 voltage value is always high	B
		Current output mode; no change in functionality or performance of OUT0	D
CAP	13	Loss of functionality; device enters short circuit protection, power consumption increases	B
AGND	14	No change in functionality or performance	D
VDD	15	Complete loss of functionality; no device damage	B
VREF	16	Loss of core DAC functionality	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB3	1	Voltage output mode; OUT3 voltage will be an incorrect value	B
		Current output mode; no change in functionality or performance of OUT3	D
OUT3	2	OUT3 output value is not available	B
OUT2	3	OUT2 output value is not available	B
FB2	4	Voltage output mode; OUT2 voltage will be an incorrect value	B
		Current output mode; no change in functionality or performance of OUT2	D
GPIO/SDO	5	Loss of GPIO functionality and read back data is not available	B
SCL/$\overline{\text{SYNC}}$	6	Loss of communication with the device	B
A0/SDI	7	Loss of communication with the device	B
SDA/SCLK	8	Loss of communication with the device	B
FB1	9	Voltage output mode; OUT1 voltage will be an incorrect value	B
		Current output mode; no change in functionality or performance of OUT1	D
OUT1	10	OUT1 output value is not available	B
OUT0	11	OUT0 output value is not available	B
FB0	12	Voltage output mode; OUT0 voltage will be incorrect value	B
		Current output mode; no change in functionality or performance of OUT0	D
CAP	13	Open;circuited pin can cause damage to the low-voltage digital core and NVM supplied by the internal LDO	A
AGND	14	Complete loss of functionality; no device damage	B
VDD	15	Complete loss of functionality; no device damage	B
VREF	16	External reference mode; loss of core DAC functionality	B
		Internal reference mode; no change in functionality or performance	D
		VDD as reference mode; no change in functionality or performance	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FB3	1	VREF	Short to corner pin is not expected	D
		OUT3	Voltage output mode; this is an intended connection	D
		OUT3	Current output mode; no change in functionality or performance of OUT3	D
OUT3	2	FB3	Voltage output mode; this is an intended connection	D
		FB3	Current output mode; no change in functionality or performance of OUT3	D
		OUT2	Device can sustain damage over a period of time	A
OUT2	3	OUT3migh	Device can sustain damage over a period of time	A
		FB2	Voltage output mode; this is an intended connection	D
		FB2	Current output mode; no change in functionality or performance of OUT2	D
FB2	4	OUT2	Voltage output mode; this is an intended connection	D
		OUT2	Current output mode; no change in functionality or performance of OUT2	D
		GPIO/SDO	Short to corner pin is not expected	D
GPIO/SDO	5	FB2	Short to corner pin is not expected	D
		SCL/$\overline{\text{SYNC}}$	Loss of communication, GPI, and SDO functionality	B
SCL/$\overline{\text{SYNC}}$	6	GPIO/SDO	Loss of communication, GPI, and SDO functionality	B
		A0/SDI	Loss of communication with the device	B
A0/SDI	7	SCL/$\overline{\text{SYNC}}$	Loss of communication with the device	B
		SDA/SCLK	Loss of communication with the device	B
SDA/SCLK	8	A0/SDI	Loss of communication with the device	B
		FB1	Short to corner pin is not expected	D
FB1	9	SDA/SCLK	Short to corner pin is not expected	D
		OUT0	Voltage output mode; this is an intended connection	D
		OUT0	Current output mode; no change in functionality or performance of OUT1	D
OUT1	10	FB1	Voltage output mode; this is an intended connection	D
		FB1	Current output mode; no change in functionality or performance of OUT1	D
		OUT0	Device can sustain damage over a period of time	A
OUT0	11	OUT1	Device can sustain damage over a period of time	A
		FB0	Voltage output mode; this is an intended connection	D
		FB0	Current output mode; no change in functionality or performance of OUT0	D
FB0	12	OUT0	Voltage output mode; this is an intended connection	D
		OUT0	Current output mode; no change in functionality or performance of OUT0	D
		CAP	Short to corner pin is not expected	D
CAP	13	FB0	Short to corner pin is not expected	D
		AGND	Device enters short circuit protection; power consumption increases	B
AGND	14	CAP	Device enters short circuit protection; power consumption increases	B
		VDD	Complete loss of functionality; no device damage	B
VDD	15	AGND	Complete loss of functionality; no device damage	B
		VREF	External reference mode; loss of core DAC functionality	B
		VREF	Internal reference mode; loss of core DAC functionality	B
		VREF	VDD as reference mode; no change in functionality or performance	D
VREF	16	VDD	External reference mode; loss of core DAC functionality	B
		VDD	Internal reference mode; loss of core DAC functionality	B
		VDD	VDD as reference mode; no change in functionality or performance	D
		FB3	Short to corner pin is not expected	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FB3	1	Voltage output mode; OUT3 voltage value is always low	B
		Current output mode; no change in functionality or performance of OUT3	D
OUT3	2	Voltage output mode - device can sustain damage over a period of time	A
		Current output mode; output compliance voltage violation and loss of performance	C
OUT2	3	Voltage output mode; device can sustain damage over a period of time	C
		Current output mode; output compliance voltage violation and loss of performance	A
FB2	4	Voltage output mode; OUT2 voltage value is always low	\B
		Current output mode; no change in functionality or performance of OUT2	D
GPIO/SDO	5	Loss of GPIO functionality and read back data will be corrupted	B
SCL/$\overline{\text{SYNC}}$	6	Loss of communication with the device	B
A0/SDI	7	Loss of communication with the device	B
SDA/SCLK	8	Loss of communication with the device	B
FB1	9	Voltage output mode; OUT1 voltage value is always low	B
		Current output mode; no change in functionality or performance of OUT1	D
OUT1	10	Voltage output mode; device can sustain damage over a period of time	A
		Current output mode; output compliance voltage violation and loss of performance	C
OUT0	11	Voltage output mode; device can sustain damage over a period of time	A
		Current output mode; output compliance voltage violation and loss of performance	C
FB0	12	Voltage output mode; OUT0 voltage value is always low	B
		Current output mode; no change in functionality or performance of OUT0	D
CAP	13	Shorting to VDD pin can cause damage to the low-voltage digital core and NVM supplied by the internal LDO	A
AGND	14	Complete loss of functionality; no device damage	B
VDD	15	No change in functionality or performance	D
VREF	16	External reference mode; loss of core DAC functionality	B
		Internal reference mode; loss of core DAC functionality	B
		VDD as reference mode; no change in functionality or performance	D

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