

# DRV8262-Q1 Functional Safety FIT Rate, FMD and Pin FMA



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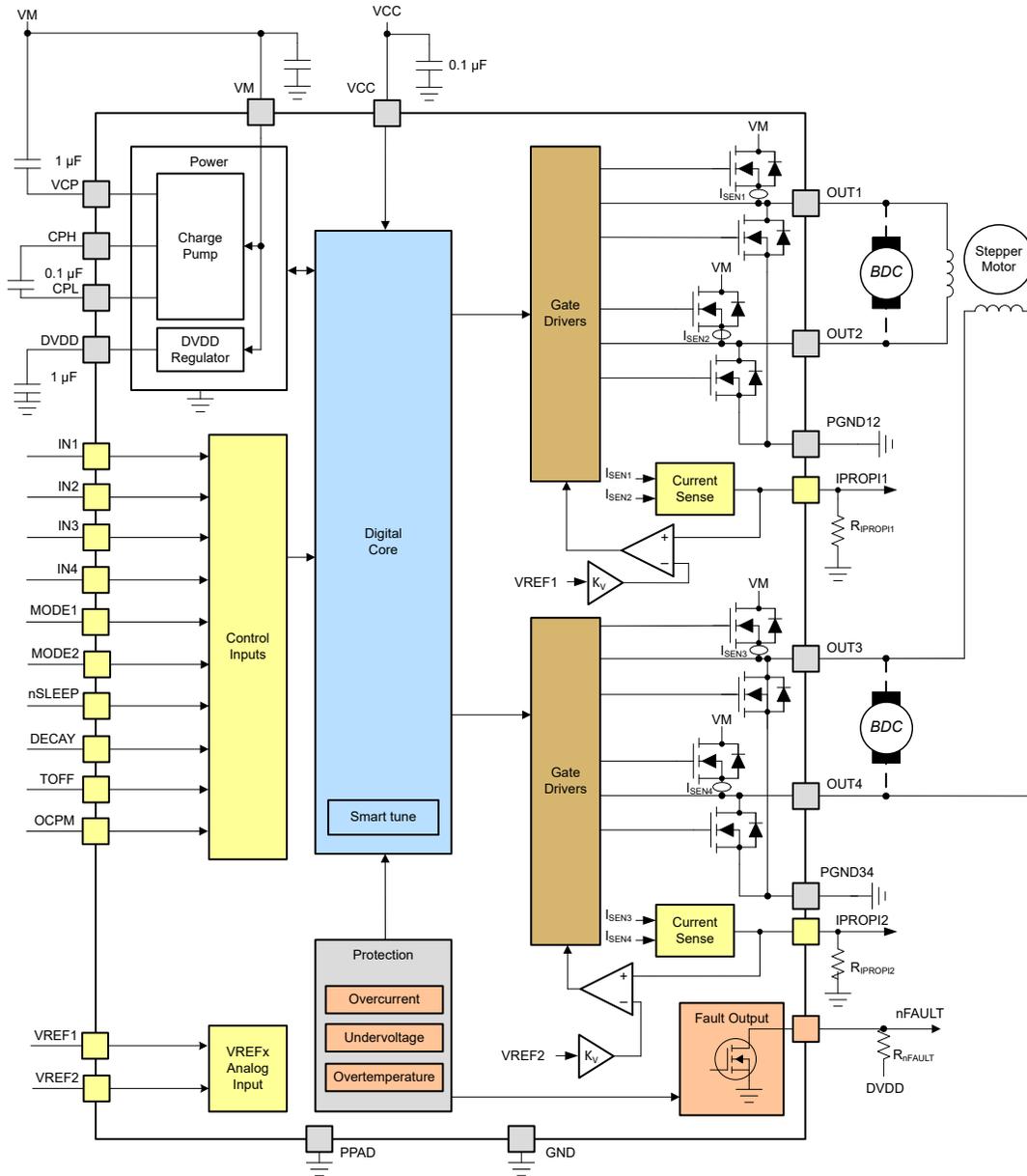
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# 1 Overview

This document contains information for the DRV8262-Q1 to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

The DRV8262-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the DRV8262-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	44
Die FIT rate	5
Package FIT rate	39

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1 W
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS/BICMOS ASICs Analog & Mixed =<50V supply	60 FIT	70°C

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the DRV8262-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution
xOUTx is stuck LOW when commanded OFF	9 %
xOUTx is stuck OFF when commanded LOW	12 %
xOUTx ON resistance too high when commanded LOW	9 %
Low side slew rate too fast or too slow	3 %
xOUTx is stuck HIGH when commanded OFF	9 %
xOUTx is stuck OFF when commanded HIGH	12 %
xOUTx ON resistance too high when commanded HIGH	9 %
High side slew rate too fast or too slow	3 %
Dead time is too short	3 %
Incorrect communication or fault indication	12 %
Current regulation incorrect	19 %

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the DRV8262-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

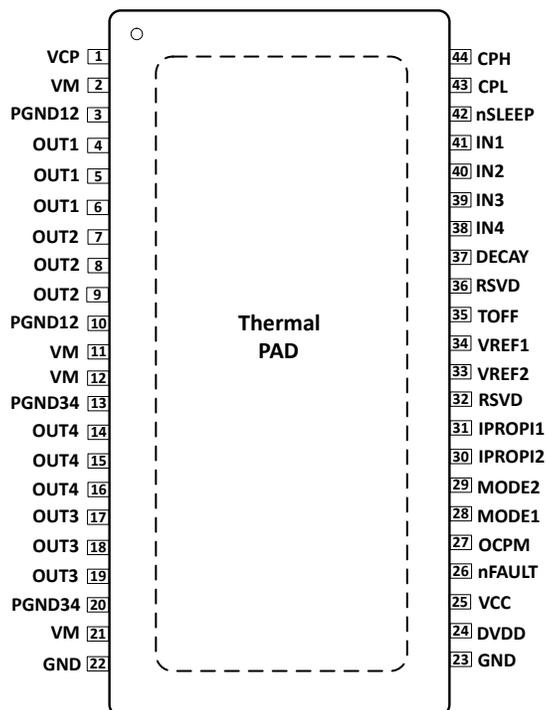
- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the DRV8262-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DRV8262-Q1 data sheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the data sheet.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCP	1	Device charge pump non-operational	A
VM	2, 11, 12, 21	Device will not power up	B
PGND12 / PGND	3, 10	Intended Operation	D
OUT1	4, 5, 6	Device will signal OCP fault	B
OUT2	7, 8, 9	Device will signal OCP fault	B
PGND34 / PGND	13, 20	Intended Operation	D
OUT4 / OUT2	14, 15, 16	Device will signal OCP fault	B
OUT3 / OUT1	17, 18, 19	Device will signal OCP fault	B
GND	22, 23	Intended Operation	D
DVDD	24	Device digital supply stuck low. Device non-operational. Drivers disabled.	B
VCC	25	Device digital supply stuck low. Device non-operational. Drivers disabled.	B
nFAULT	26	Device will always be signaling fault	B
OCPM	27	Device only works with latch-off type recovery for OCP and OTSD	B
MODE1	28	Device only works in Dual H-bridge mode	B
MODE2	29	Device only works in PH/EN mode	B
IPROPI2 / IPROPI	30	Current sense output will not be available	B
IPROPI1 / IPROPI	31	Current sense output will not be available	B
RSVD	32, 36	No impact to functionality	D
VREF2 / VREF	33	Current regulation will be lost	B
VREF1 / VREF	34	Current regulation will be lost	B
TOFF	35	OFF time will be permanently set at 7 us	B
DECAY	37	Device will work only with slow decay	B
IN4	38	OUT4 will be stuck low	B
IN3	39	OUT3 will be stuck low	B
IN2	40	OUT2 will be stuck low	B
IN1	41	OUT1 will be stuck low	B
nSLEEP	42	Device will be in sleep state with OUTx Hi-Z	B
CPL	43	Device charge pump non-operational	B
CPH	44	Device charge pump non-operational	A

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCP	1	Device charge pump non-operational	B
VM	2, 11, 12, 21	Device will not power up	B
PGND12 / PGND	3, 10	Device will not power up	B
OUT1	4, 5, 6	Device will not be able to drive the load properly	B
OUT2	7, 8, 9	Device will not be able to drive the load properly	B
PGND34 / PGND	13, 20	Device will not power up	B
OUT4 / OUT2	14, 15, 16	Device will not be able to drive the load properly	B
OUT3 / OUT1	17, 18, 19	Device will not be able to drive the load properly	B
GND	22, 23	Device will not power up	B
DVDD	24	Device digital supply missing. Device non-operational.	B
VCC	25	Device digital supply missing. Device non-operational.	B
nFAULT	26	Fault signaling will be lost	B
OCPM	27	Device only works with latch-off type recovery for OCP and OTSD	B
MODE1	28	Device only works in dual H-bridge mode	B
MODE2	29	Device only works in PWM mode	B
IPROPI2 / IPROPI	30	Current sense output will not be available	B
IPROPI1 / IPROPI	31	Current sense output will not be available	B
RSVD	32, 36	No impact to functionality	D
VREF2 / VREF	33	Current regulation will be lost	B
VREF1 / VREF	34	Current regulation will be lost	B
TOFF	35	OFF time will be permanently set at 24us	B
DECAY	37	Device will work only with mixed decay	B
IN4	38	PWM functionality will not be available for OUT4	B
IN3	39	PWM functionality will not be available for OUT3	B
IN2	40	PWM functionality will not be available for OUT2	B
IN1	41	PWM functionality will not be available for OUT1	B
nSLEEP	42	Device will be in sleep state with OUTx Hi-Z	B
CP	43	Device charge pump non-operational	B
CPH	44	Device charge pump non-operational	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCP	1	2	Device charge pump non-operational	B
VM	2	3	Device will not power up	B
PGND12	3	4	Device will signal OCP fault	B
OUT1	4	5	Intended Operation	D
OUT1	5	6	Intended Operation	D
OUT1	6	7	Device will signal OCP fault	B
OUT2	7	8	Intended Operation	D
OUT2	8	9	Intended Operation	D
OUT2	9	10	Device will signal OCP fault	B
PGND12	10	11	Device will not power up	B
VM	11	12	Intended Operation	D
VM	12	13	Device will not power up	B
PGND34	13	14	Device will signal OCP fault	B
OUT4	14	15	Intended Operation	D
OUT4	15	16	Intended Operation	D
OUT4	16	17	Device will signal OCP fault	B
OUT3	17	18	Intended Operation	D
OUT3	18	19	Intended Operation	D
OUT3	19	20	Device will signal OCP fault	B
PGND34	20	21	Device will not power up	B
VM	21	22	Device will not power up	B
GND	22	23	Intended Operation	D
GND	23	24	Digital supply missing. Device non-operational.	B
DVDD	24	25	Digital supply missing. Device non-operational.	B
VCC	25	26	Device will reset whenever nFAULT is asserted low	B
nFAULT	26	27	OCP/OTSD recovery setting and fault signal will be lost	B
OCPM	27	28	OCP/OTSD recovery and MODE setting will be lost	B
MODE1	28	29	MODE setting will be lost	B
MODE2	29	30	MODE setting and current sense output function will be lost	B
IPROP12	30	31	Current sense output functionality will be lost	B
IPROP11	31	32	No impact to functionality	D
RSVD	32	33	No impact to functionality	D
VREF2	33	34	Independent current regulation will be non-functional	B
VREF1	34	35	Current regulation and off time setting will be non-functional	B
TOFF	35	36	No impact to functionality	D
RSVD	36	37	No impact to functionality	D
DECAY	37	38	Decay mode setting and input PWM function will be lost	B
IN4	38	39	Input PWM functionality will be lost	B
IN3	39	40	Input PWM functionality will be lost	B
IN2	40	41	Input PWM functionality will be lost	B
IN1	41	42	Input PWM and Sleep mode function will be lost	B
nSLEEP	42	43	Device charge pump non-operational	A
CPL	43	44	Device charge pump non-operational	B
CPH	44	1	Device charge pump non-operational	B

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCP	1	Device charge pump non-operational	B
VM	2, 11, 12, 21	Intended Operation	D
PGND12 / PGND	3, 10	Device will not power up	B
OUT1	4, 5, 6	Device will signal OCP fault	B
OUT2	7, 8, 9	Device will signal OCP fault	B
PGND34 / PGND	13, 20	Device will not power up	B
OUT4 / OUT2	14, 15, 16	Device will signal OCP fault	B
OUT3 / OUT1	17, 18, 19	Device will signal OCP fault	B
GND	22, 23	Device will not power up	B
DVDD	24	Low voltage pin maximum voltage violated	A
VCC	25	Low voltage pin maximum voltage violated	A
nFAULT	26	Low voltage pin maximum voltage violated	A
OCPM	27	Low voltage pin maximum voltage violated	A
MODE1	28	Low voltage pin maximum voltage violated	A
MODE2	29	Low voltage pin maximum voltage violated	A
IPROPI2 / IPROPI	30	Low voltage pin maximum voltage violated	A
IPROPI1 / IPROPI	31	Low voltage pin maximum voltage violated	A
RSVD	32, 36	Low voltage pin maximum voltage violated	A
VREF2 / VREF	33	Low voltage pin maximum voltage violated	A
VREF1 / VREF	34	Low voltage pin maximum voltage violated	A
TOFF	35	Low voltage pin maximum voltage violated	A
DECAY	37	Low voltage pin maximum voltage violated	A
IN4	38	Low voltage pin maximum voltage violated	A
IN3	39	Low voltage pin maximum voltage violated	A
IN2	40	Low voltage pin maximum voltage violated	A
IN1	41	Low voltage pin maximum voltage violated	A
nSLEEP	42	Driver control will be lost	B
CPL	43	Device charge pump non-operational	A
CPH	44	Device charge pump non-operational	B

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