Functional Safety Information

LM63635C-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LM63635C-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

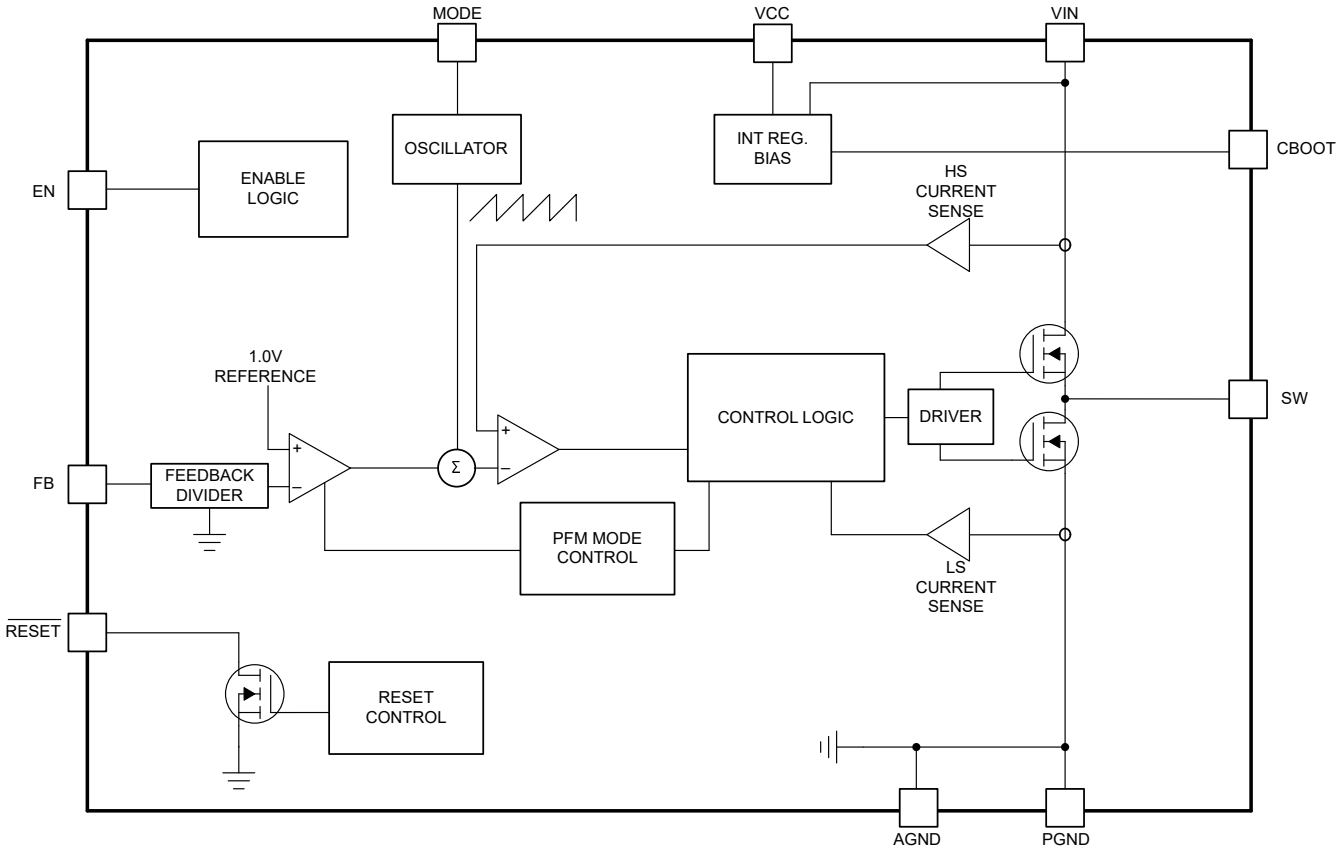

Figure 1-1. Functional Block Diagram

The LM63635C-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM63635C-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	6
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 600mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55ºC

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM63635C-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35
SW output not in specification - voltage or timing	45
SW driver FET stuck on	10
RESET false trip or fails to trip	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM63635C-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM63635C-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM63635C-Q1 data sheet.

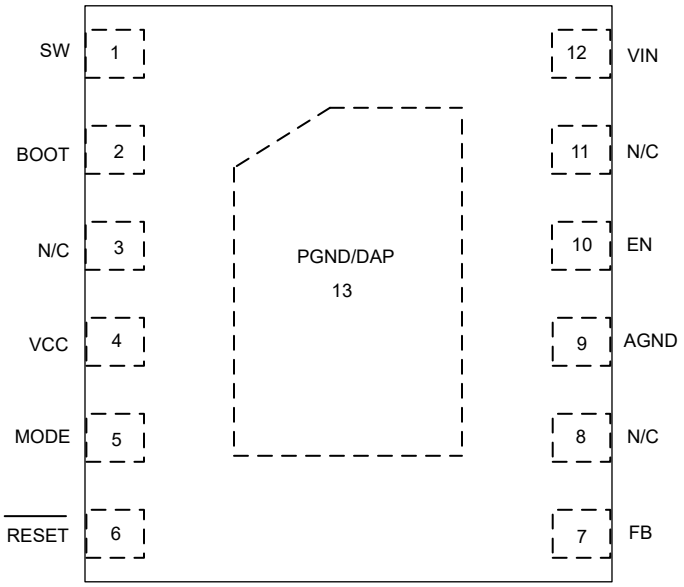

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the 'Recommended Operating Conditions' and the 'Absolute Maximum Ratings' found in LM63635C-Q1 data sheet.
- The typical application circuit, as per the LM63635C-Q1 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	2	Damage to internal circuits	A
N/C	3	No effect	D
VCC	4	Fault mode shuts the device off.	B
MODE	5	No effect	D
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ functionality is lost.	B
FB	7	The regulator operates at the maximum duty cycle. The output voltage rises to nearly the input voltage (V_{IN}) level. Possible damage to customer load, output stage components, or both, can occur. No effect on the device.	B
N/C	8	No effect	D
AGND	9	No effect	D
EN	10	Loss of ENABLE functionality The device remains in shutdown mode.	B
N/C	11	No effect	D
VIN	12	The device does not operate. No output voltage is generated. Output capacitors discharge through input short. Large reverse current can damage device.	A
PGND	13	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	Loss of output voltage	B
BOOT	2	Loss of output voltage regulation; low or no output voltage. Damage to the internal device.	A
N/C	3	No effect	D
VCC	4	VCC LDO is unstable. Loss of output voltage regulation and possible damage to internal circuits.	A
MODE	5	No effect	D
$\overline{\text{RESET}}$	6	Loss of $\overline{\text{RESET}}$ functionality	B
FB	7	Loss of output voltage regulation. Output voltage can rise or fall outside of intended regulation window. Possible damage to the customer load.	B
N/C	8	No effect	D
AGND	9	Loss of output voltage regulation. Possible damage to the internal circuits.	A
EN	10	Loss of ENABLE functionality. Erratic operation; probable loss of regulation	B
N/C	11	No effect	D
VIN	12	Loss of output voltage	B
PGND	13	Possible device damage	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SW	1	BOOT	Loss of output regulation, possible damage to internal circuits	A
BOOT	2	N/C	No effect	D
N/C	3	VCC	No effect	D
VCC	4	MODE	Not switching in auto mode at light load.	B
MODE	5	$\overline{\text{RESET}}$	Possible damage to device internal circuits	A
FB	7	N/C	No effect	D
N/C	8	AGND	No effect	D
AGND	9	EN	Loss of enable function. The devices shut down.	B
EN	10	N/C	No effect	D
N/C	11	VIN	No effect	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	2	Damage to internal circuits	A
N/C	3	No effect	D
VCC	4	Damage to internal circuits for V_{IN} > 5.5V	A
MODE	5	Damage to internal circuits	A
$\overline{\text{RESET}}$	6	Damage to internal circuits	A
FB	7	Damage to internal circuits	A
N/C	8	No effect	D
AGND	9	Possible damage to internal circuits or package	A
EN	10	No damage to device. Loss of ENABLE functionality	B
N/C	11	No effect	D
VIN	12	No effect	D
PGND	13	Possible damage to internal circuits or package	A

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