Functional Safety Information

UCC27624-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the UCC27624-Q1 (D, DGN, and DSD packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

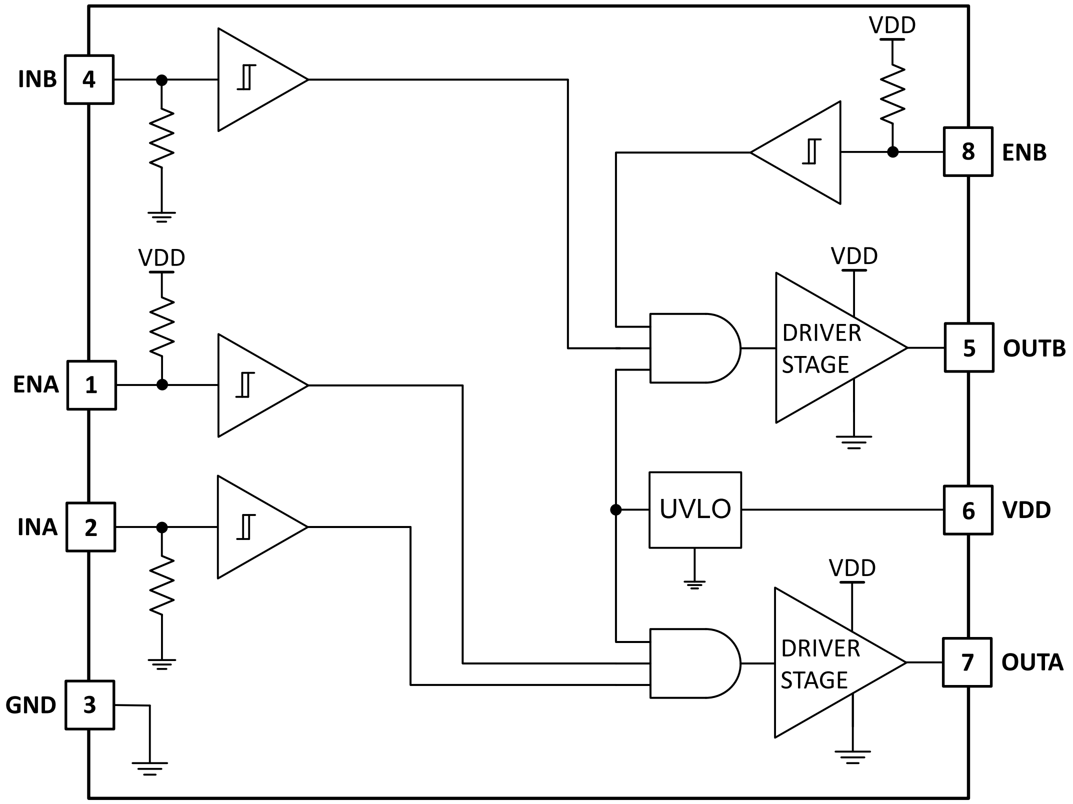

Figure 1-1. Functional Block Diagram

The UCC27624-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 D Package

This section provides functional safety failure in time (FIT) rates for the D package of the UCC27624-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	5
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DGN Package

This section provides functional safety failure in time (FIT) rates for the DGN package of the UCC27624-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	5
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 DSD Package

This section provides functional safety failure in time (FIT) rates for the DGN package of the UCC27624-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	6
Package FIT rate	4

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC27624-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTA stuck low	8
OUTB stuck low	8
OUTA stuck high	8
OUTB stuck high	8
OUTA unknown	8
OUTB unknown	8
UVLO stuck low	2
UVLO stuck high	2
UVLO unknown	2
ENA stuck high	1
ENA stuck low	1
ENA unknown	1
Others, no impact	43

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC27624-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1, Figure 4-2, and Figure 4-3 show the UCC27624-Q1 pin diagrams. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC27624-Q1 data sheet.

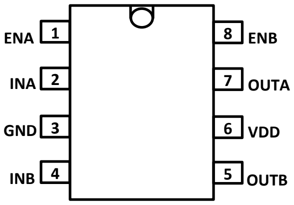

Figure 4-1. D Package Pin Diagram

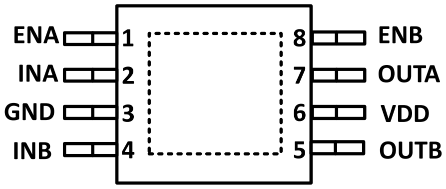

Figure 4-2. DGN Package Pin Diagram

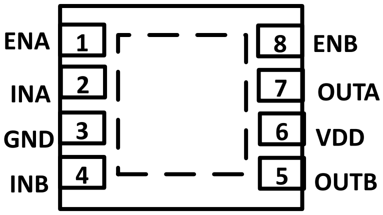

Figure 4-3. DSD Package Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin 1 shorted to pin 8 and pin 4 shorted to pin 5 are not considered.
- The case of a short-circuit to supply is analyzed as a short to VDD.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	The ENA function is disabled. OUTA does not respond to INA.	B
INA	2	The INA function is lost. OUTA is stuck low.	B
GND	3	No impact.	D
INB	4	The INB function is lost. OUTB is stuck low.	B
OUTB	5	OUTB is stuck low. OUTB is short circuited if INB is commanded *High*.	A
VDD	6	There is a VDD undervoltage. OUTA and OUTB are off.	B
OUTA	7	OUTA is stuck low. OUTA is short circuited if INA is commanded *High*.	A
ENB	8	The ENB function is disabled. OUTB does not respond to INB.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	OUTA is always enabled. OUTA responds to INA.	B
INA	2	The INA function is lost. OUTA is stuck low.	B
GND	3	The state of OUTA and OUTB are unknown.	B
INB	4	The INB function is lost. OUTB is stuck low.	B
OUTB	5	OUTB is disconnected from the power FET.	B
VDD	6	There is a VDD undervoltage. OUTA and OUTB are off.	B
OUTA	7	OUTA is disconnected from the power FET.	B
ENB	8	OUTB is always enabled. OUTB responds to INB.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ENA	1	INA	ENA cannot override the INA command. OUTA responds to INA.	B
INA	2	GND	OUTA is stuck low.	B
GND	3	INB	OUTB is stuck low.	B
OUTB	5	VDD	OUTB is stuck high.	A
VDD	6	OUTA	OUTA is stuck high.	A
OUTA	7	ENB	The ENB function depends on the state of INA (OUTA).	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	OUTA is always enabled. OUTA responds to INA.	B
INA	2	OUTA is stuck high.	B
GND	3	The power supply is short circuited.	B
INB	4	OUTB is stuck high.	B
OUTB	5	OUTB is stuck high.	A
VDD	6	No impact.	D
OUTA	7	OUTA is stuck high.	A
ENB	8	OUTB is always enabled. OUTB responds to INB	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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