

OPA4376-Q1 Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	3
3 Failure Mode Distribution (FMD).....	4
4 Pin Failure Mode Analysis (Pin FMA).....	5

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for the OPA4376-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

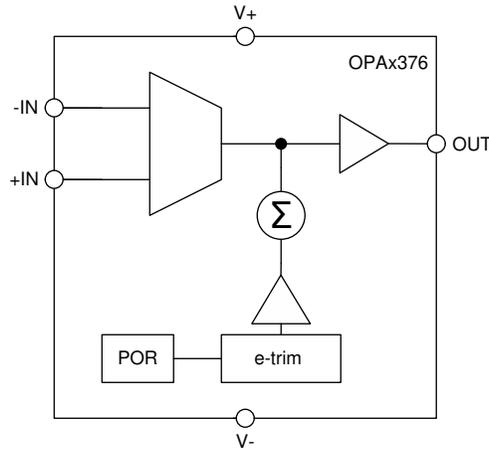


Figure 1-1. Functional Block Diagram

The OPA4376-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the OPA4376-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	10
Die FIT rate	2
Package FIT rate	8

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 10.45 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the OPA4376-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20
Output saturated high	25
Output saturated low	25
Output functional, not in specification voltage or timing	30

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the OPA4376-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the OPA4376-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the OPA4376-Q1 data sheet.

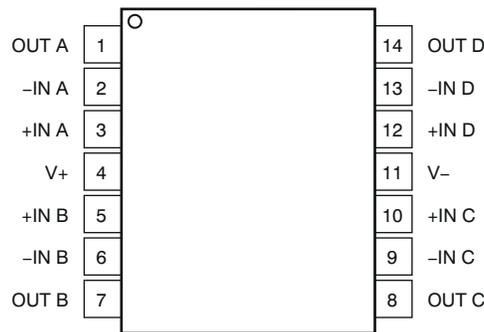


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 'Short circuit to Power' means short to V+.
- 'Short circuit to GND or Ground' means short to V-.
- V+ is equivalent to VCC and V- equivalent to VEE.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V ₋ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
-IN A	2	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
V+	4	Op-amp supplies are shorted together, leaving the V+ pin at some voltage between the V+ and V ₋ sources (depending on the source impedance).	A
+IN B	5	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
-IN B	6	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V ₋ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
OUT C	8	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT C voltage ultimately forced to the V ₋ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
-IN C	9	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
+IN C	10	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN D	12	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
-IN D	13	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
OUT D	14	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT D voltage ultimately forced to the V ₋ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	No negative feedback or ability for OUT A to drive the application.	B
–IN A	2	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
+IN A	3	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
V+	4	Positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	A
+IN B	5	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
–IN B	6	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
OUT B	7	No negative feedback or ability for OUT B to drive the application.	B
OUT C	8	No negative feedback or ability for OUT C to drive the application.	B
–IN C	9	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN C pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
+IN C	10	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN C pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
V–	11	Negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
+IN D	12	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output likely ends up at the positive or negative rail. The +IN D pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
–IN D	13	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN D pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
OUT D	14	No negative feedback or ability for OUT D to drive the application.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	2	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	B
-IN A	2	3	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
+IN A	3	4	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to +IN A.	B
V+	4	5	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to V+.	B
+IN B	5	6	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
-IN B	6	7	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	B
OUT B	7	8	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the OUT C voltage or vice versa. Prolonged exposure to short-circuit conditions might result in long-term reliability issues.	A
OUT C	8	9	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	B
-IN C	9	10	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
+IN C	10	11	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
V-	11	12	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
+IN D	12	13	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
-IN D	13	14	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	B
OUT D	14	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT D voltage ultimately forced to the OUT A voltage or vice versa. Prolonged exposure to short-circuit conditions might result in long-term reliability issues.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT A voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
-IN A	2	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to +IN A.	B
+IN B	5	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to +IN B.	B
-IN B	6	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
OUT C	8	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT C voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
-IN C	9	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
+IN C	10	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to +IN C.	B
V-	11	Op-amp supplies are shorted together, leaving the V- pin at some voltage between the V- and V+ sources (depending on the source impedance).	A
+IN D	12	Depending on the circuit configuration, the application is likely not to function because device common-mode voltage is connected to +IN D.	B
-IN D	13	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
OUT D	14	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT D voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated