Functional Safety Information

LMR36500 Functional Safety FIT Rate, FMD and Pin FMA

TEXAS INSTRUMENTS

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1 Overview

This document contains information for LMR36500 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

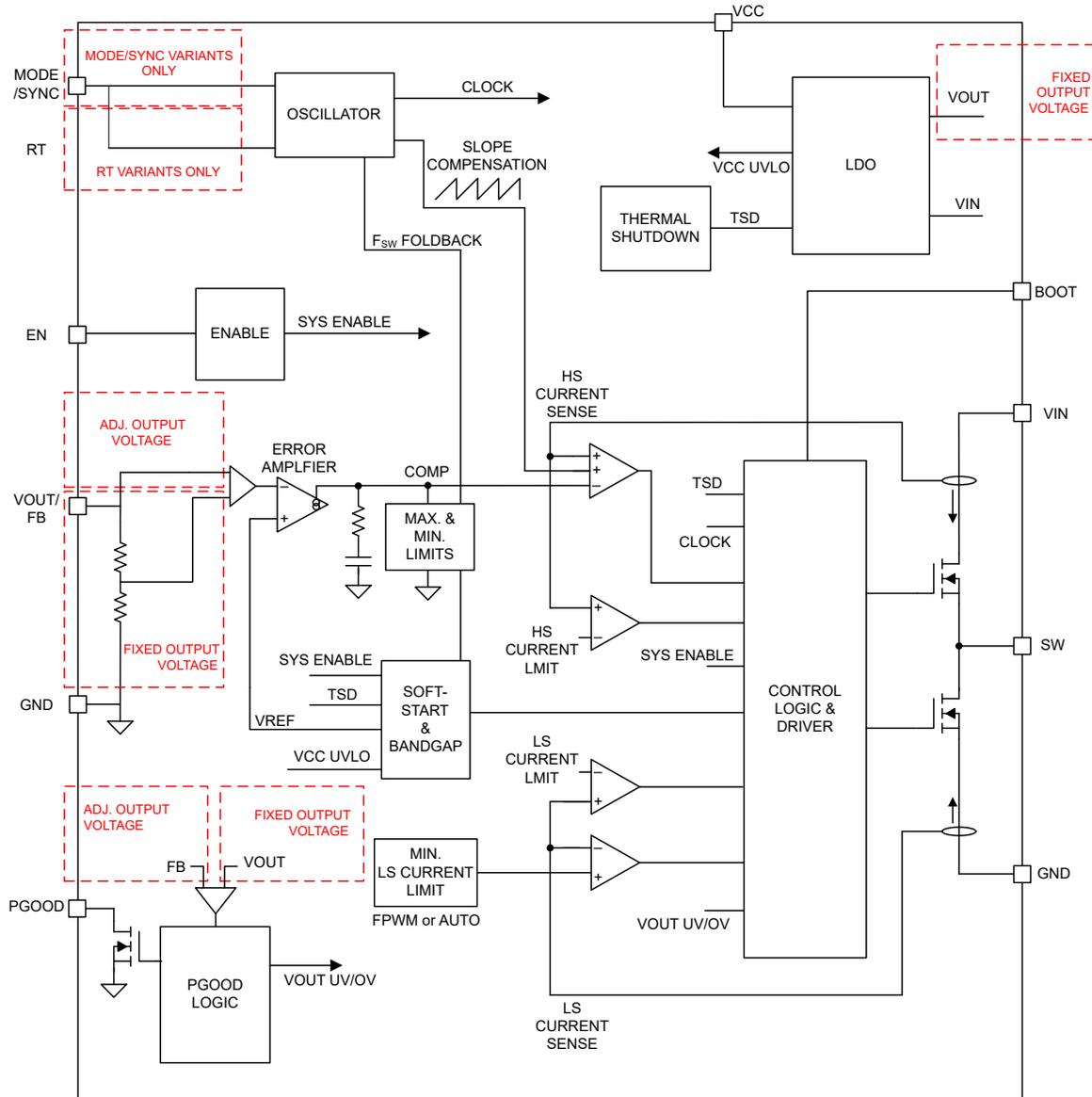Figure 1-1 shows the device functional block diagram for reference.

Figure 1-1. Functional Block Diagram

LMR36500 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates
2.1 LMR36500

This section provides Functional Safety Failure In Time (FIT) rates for LMR36500 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 35 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/ BICMOS ASICs Analog & Mixed HV >50V supply	30 FIT	75°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR36500 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	60%
Output not in specification - voltage or timing	30%
Gate Driver stuck on	5%
Power Good - False Trip or Failure to Trip	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR36500. The failure modes covered in this document include the typical pin-by-pin failure scenarios:
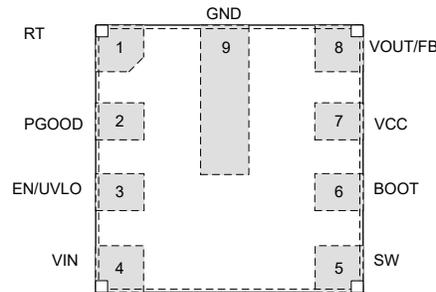
- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LMR36500 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR36500 data sheet.

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RT	1	Switching Frequency is 2.2 MHz	D
PGOOD	2	When not in use can be left grounded (PGOOD is not a valid signal, VOUT normal)	D
EN/UVLO	3	VOUT = 0 V (Enable is off, functionality is halted)	D
VIN	4	VOUT = 0 V	B
SW	5	Damage HSFET	A
BOOT	6	VOUT = 0 V, HS will not turn on	B
VCC	7	VOUT = 0 V	B
VOUT/FB	8	VOUT = 0 V	B
GND	9	VOUT normal	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RT	1	Frequency will not be defined.	C
PGOOD	2	When not in use, can be left open (PGOOD is not a valid signal, VOUT normal)	D
EN/UVLO	3	Pin cannot be left floating	B
VIN	4	VOUT = 0 V	B
SW	5	VOUT = 0 V	B
BOOT	6	VOUT = 0, HS will not turn on	B
VCC	7	VCC output will be unstable, can increase above 5.5 V	A
VOUT/FB	8	VOUT will be abnormal. Do not float this pin.	C
GND	9	VOUT can be abnormal, as reference voltage is not fixed	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
RT	1	PGOOD	If PGOOD is high, and less than 5.5 V Fsw = 1 MHz; If PGOOD is low, Fsw = 2.2 MHz. RT pin will become damaged if PG exceeds 5.5 V.	A
PGOOD	2	EN/UVLO	If EN/UVLO > 20 V, it will damage devices connected to PGOOD pin.	A
EN/UVLO	3	VIN	VOUT normal (Enable is on, all other blocks will work)	D
VIN	4	SW	Damage LSFET	A
SW	5	BOOT	VOUT = 0 V, HS will not turn on, no Cboot	B
BOOT	6	VCC	Damage will occur, break VCC Pin	A
VCC	7	VOUT/FB	If VOUT/FB votlage is less than 5.5 V, then no damage will occur.	B
VOUT/BIAS or FB	8	GND	VOUT = 0 V	B
GND	9	RT or MODE	If RT pin is already low, then the part is functional. Otherwise abnormal behavior. No damage to part.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RT	1	If Vin > 5.5 V, damage will occur. If Vin < 5.5 V, refer to the data sheet.	A
PGOOD	2	If VIN > 20 V, damage will occur.	A
EN/UVLO	3	VOUT normal (Enable is on, all other blocks will work).	D
VIN	4	VOUT normal.	D
SW	5	Damage LSFET.	A
BOOT	6	Damage will occur, BOOT ESD clamp will be damaged.	A
VCC	7	If Vin > 5.5, damage will occur.	A
VOUT/FB	8	If VIN > 16 V, damage will occur.	A
GND	9	VOUT = 0 V	B

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