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## 1 Overview

This document contains information for LMR38015-Q1, LMR38025-Q1 ( WSON (12) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

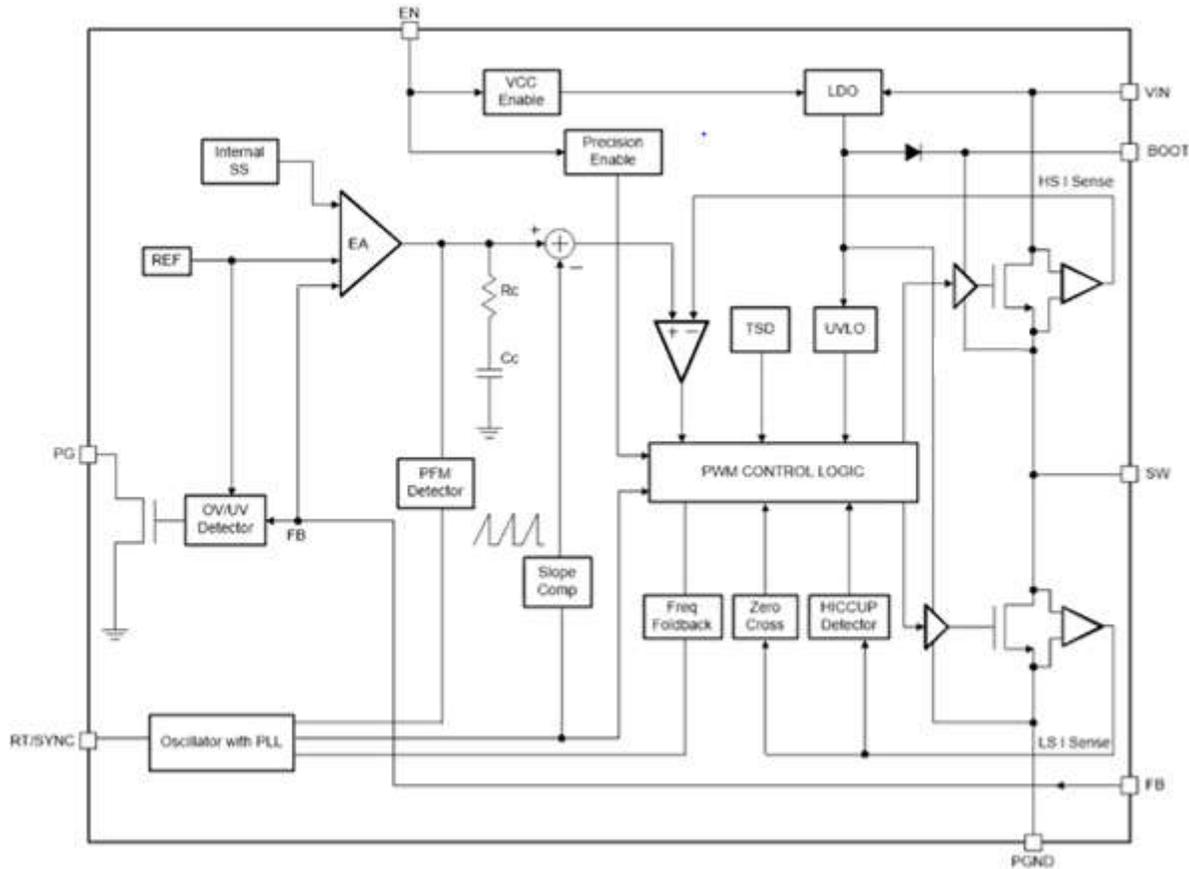


Figure 1-1. Functional Block Diagram

LMR38015-Q1, LMR38025-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LMR38015-Q1, LMR38025-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	10
Die FIT Rate	5
Package FIT Rate	5

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1000mW
- Climate type: World-wide Table 8
- Package factor ( $\lambda_3$ ): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS/BICMOS ASICs Analog & Mixed HV >50V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR38015-Q1, LMR38025-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
No SW output	50
SW output not in specification – voltage or timing	40
SW power FET stuck on	5
PGOOD false trip, fails to trip	5

The FMD in [Table 3-1](#) excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR38015-Q1, LMR38025-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

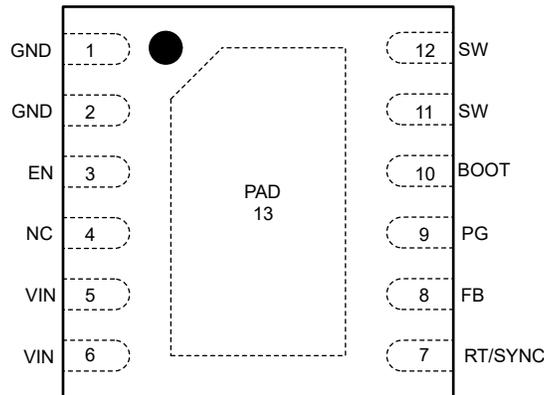
- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the LMR38015-Q1, LMR38025-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR38015-Q1, LMR38025-Q1 data sheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LMR38015-Q1, LMR38025-Q1 datasheet

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1/2	Normal operation	D
EN	3	VOUT = 0 V	B
VIN	5/6	VOUT = 0 V	B
RT/SYNC	7	Switching Frequency >> 3 MHz	C
FB	8	VOUT >> than programmed output voltage	B
PG	9	No power good function	B
BOOT	10	VOUT = 0 V	B
SW	11/12	Damage to HS FET	A

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1/2	VOUT might be abnormal due to switching noise on analog circuits	B
EN	3	Device can shut off	B
VIN	5/6	Device can shut off	B
RT/SYNC	7	No Switching frequency	B
FB	8	VOUT >> than programmed output voltage	B
PG	9	No power good function	B
BST	10	VOUT = 0 V	B
SW	11/12	VOUT = 0 V	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name 1	Pin Name 2	Description of Potential Failure Effect(s)	Failure Effect Class
GND	EN	VOUT = 0 V	B
EN	VIN	Normal Vout operation	B
FB	PG	VOUT less than programmed output voltage	B
PG	BOOT	PGOOD Pin ESD damage if BOOT pin voltage >20 V	A
BOOT	SW	VOUT = 0 V	B

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1/2	VOUT = 0 V. Damage to other pins referred to GND.	A
EN	3	Device enabled	D
VIN	5/6	Normal mode	D
RT/SYNC	7	RT/SYNC Pin ESD damage if VIN > 5.5 V	A
FB	8	If VIN exceeds 5.5 V damage will occur. VOUT = 0 V	A
PG	9	PGOOD Pin ESD damage if VIN >20V	B
BOOT	10	VOUT = 0 V. CBOOT ESD clamp will run current to destruction	A
SW	11/12	Damage to LS FET	A

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