Functional Safety Information

TPS22995H-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPS22995H-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

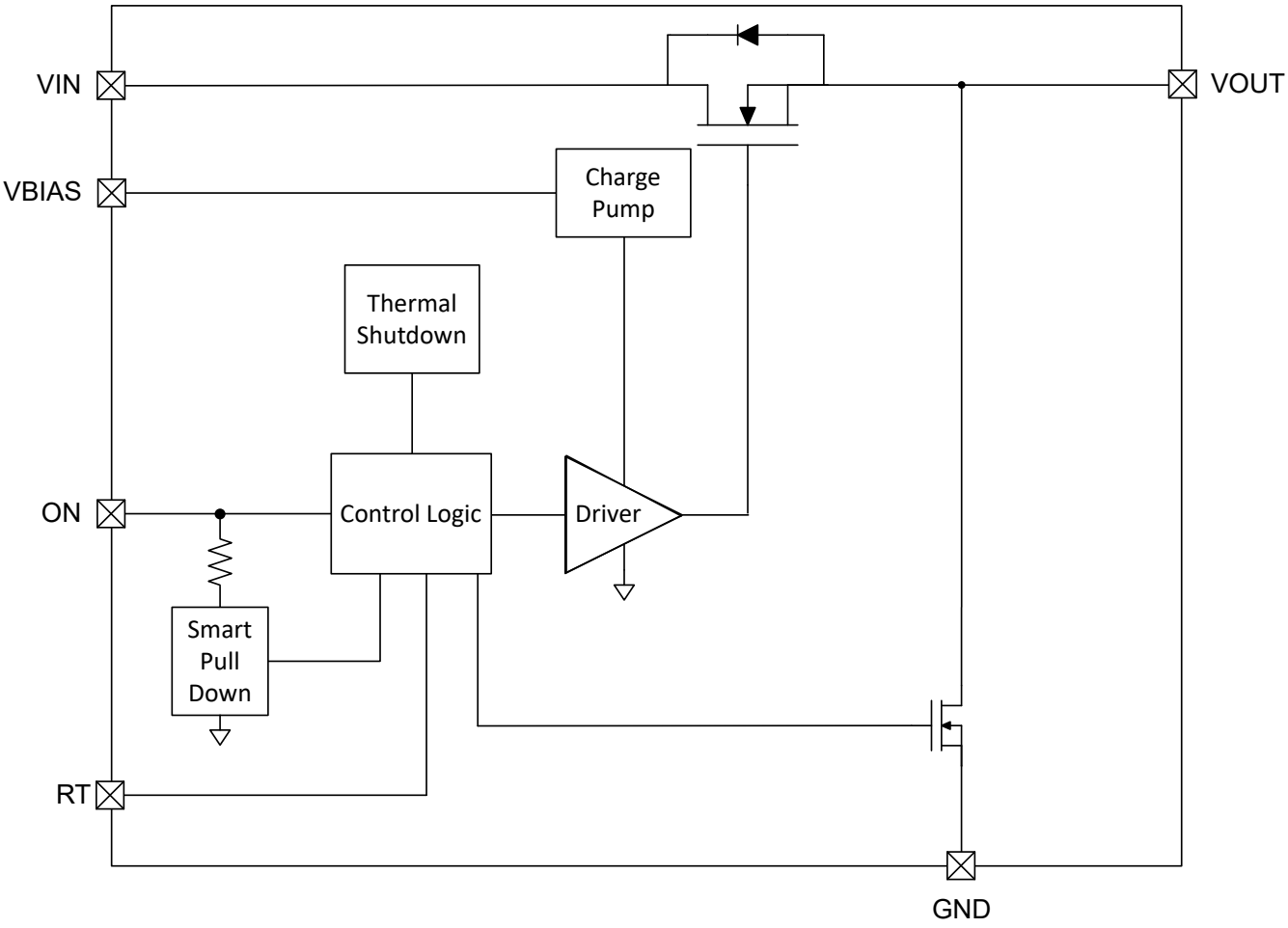

Figure 1-1. Functional Block Diagram

TPS22995H-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS22995H-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	3
Package FIT rate	3

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 171mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS22995H-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open or Hi-Z	25
VOUT stuck on (VIN)	15
VOUT outside specification (voltage or rise time)	45
QOD stuck on	5
QOD stuck off	5
Pin to pin short (any two pins)	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS22995H-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS22995H-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS22995H-Q1 data sheet.

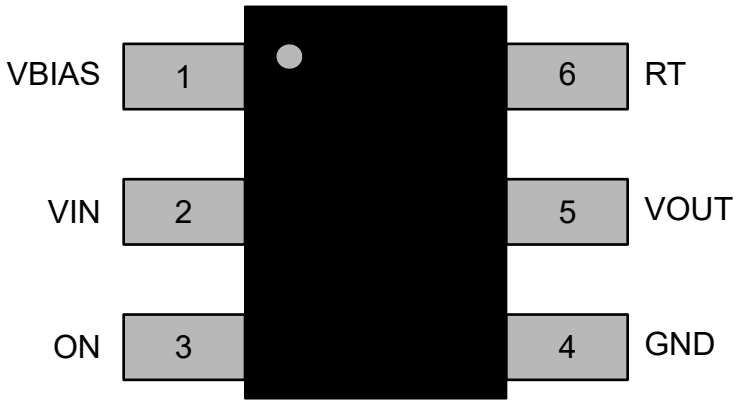

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device pins are connected per the recommendation in the data sheet, including pullup and pulldown resistors, as needed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VBIAS	1	No power supply to the device. The device does not pass through voltage to VOUT.	B
VIN	2	The power supply is shorted.	D
ON	3	The device is disabled.	D
GND	4	This is the GND pin. Normal operation.	D
VOUT	5	If the device is enabled, the device does not limit the power supply current and is damaged.	A
RT	6	Grounding this pin quickens the output rise time more than expected if an RT resistor is connected or the pin is intended to be left open.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VBIAS	1	No power supply to the device. The device does not pass through voltage to VOUT.	B
VIN	2	No power supply to the device. The device does not pass through voltage to VOUT.	D
ON	3	The ON pin can float high or low, the output state is unknown.	D
GND	4	No GND connection to the device. Not functional.	D
VOUT	5	The output does not deliver the voltage to the load.	D
RT	6	Opening this pin slows down the output rise time more than expected if an RT resistor is attached or the pin is intended to be grounded.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VBIAS	1	VIN	A stronger supply powers the IN and BIAS pins. Device operation can be affected, no device damage.	D
VIN	2	ON	The device is enabled if the VIN power supply is above the ON threshold (VIH).	D
GND	4	VOUT	If the device is enabled, the device does not limit the power supply current and is damaged.	A
VOUT	5	RT	Shorting this pin quickens the output rise time more than expected if an RT resistor is attached.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VBIAS	1	Normal operation is expected.	D
VIN	2	Normal operation is expected.	D
ON	3	The device is enabled if the power supply is above the ON threshold (VIH).	D
GND	4	The power supply is shorted.	D
VOUT	5	The power MOSFET is shorted. Disabling the device no longer blocks power to VOUT.	B
RT	6	The output rise time slows down.	C

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

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