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1 Overview

This document contains information for LM749x0-Q1 to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device

Figure 1-1 shows the device functional block diagram for reference.

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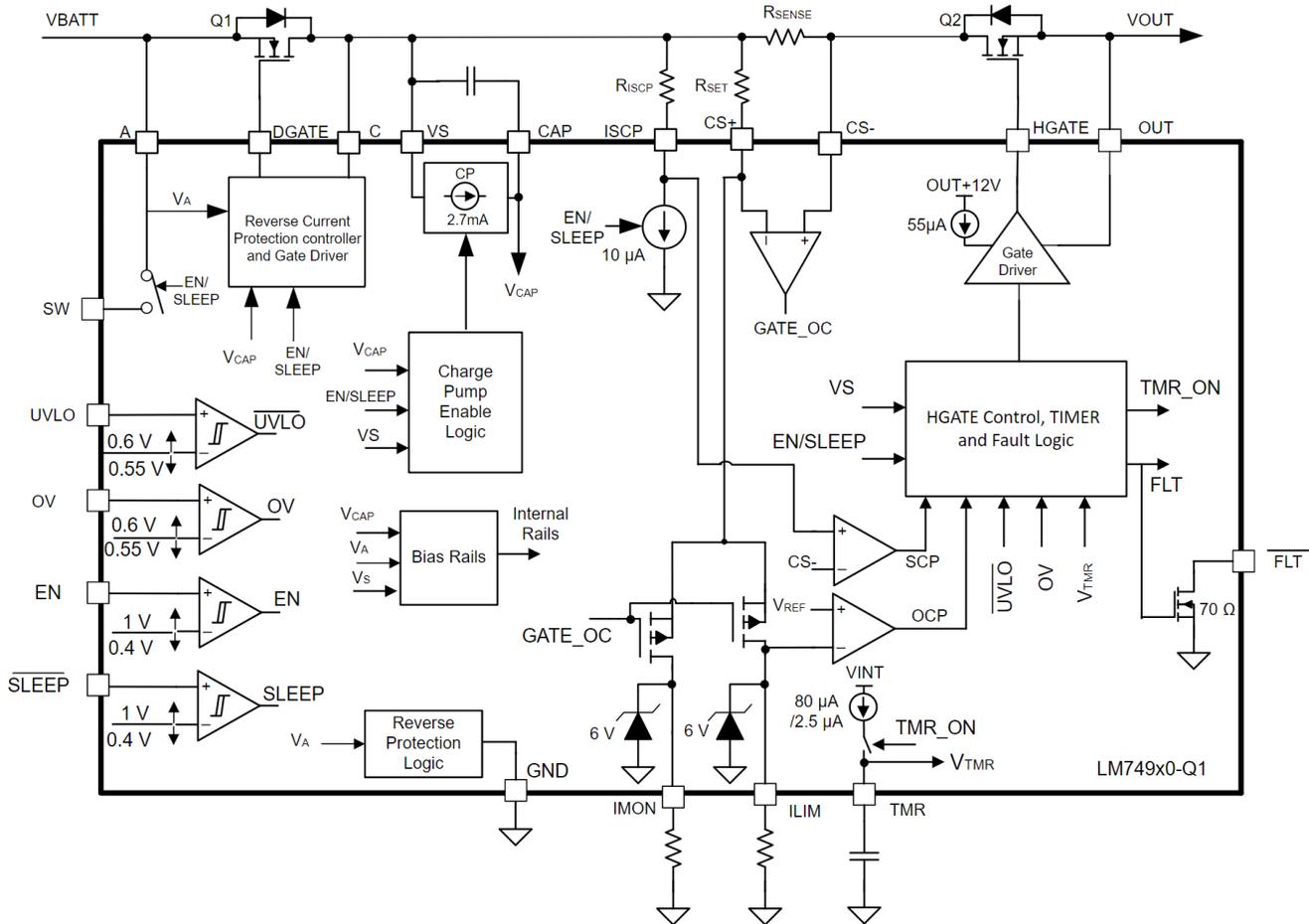


Figure 1-1. Functional Block Diagram

LM749x0-Q1 is developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM749x0-Q1 (LM74900-Q1, LM74910-Q1) based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	14
Die FIT Rate	3
Package FIT Rate	11

The failure rate and mission profile information in [Table 2-2](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 42mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS logic	25	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM749x0-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DGATE stuck at low	20%
DGATE voltage or timing not in specification	20%
HGATE stuck at low	25%
HGATE voltage or timing not in specification	25%
OUT voltage or timing not in specification	5%
Pin to Pin short	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM74900-Q1, LM74910-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the LM749x0-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM749x0-Q1 data sheet.

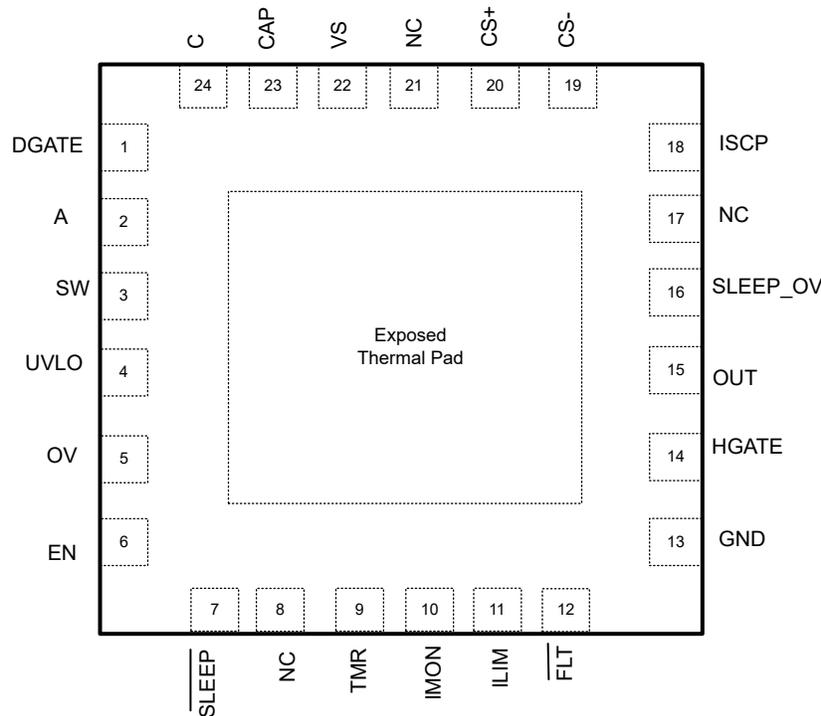


Figure 4-1. Pin Diagram

The pin FMA is provided under the assumption that the device is operating under the specified ranges within the Recommended Operating Conditions section of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	Device is damaged due to internal conduction. External DGATE FET can also damage due to maximum VGS rating violation.	A
A	2	Input supply shorted to ground. Device not functional.	B
SW	3	Device is damaged if enabled.	A
UVLO	4	Device HGATE drive is off.	B
OV	5	Overvoltage protection functionality is disabled.	B
EN	6	Device is in shutdown mode.	B
SLEEP	7	Device is in SLEEP mode.	B
N.C	8, 17, 21	No effect on device operation.	D
TMR	9	Timer functionality is not be available.	B
IMON	10	Current monitoring output is not available.	B
ILIM	11	Overcurrent protection with circuit breaker feature is not be available.	B
FLT	12	Fault indication functionality is not be available.	B
GND	13	No impact on the device functionality.	D
HGATE	14	Device is damaged.	A
OUT	15	External FET VGS(max) rating can exceed and damage external FET. Device can experience increase in quiescent current.	D
SLEEP_OV	16	Overvoltage protection during SLEEP mode is not available.	B
ISCP	18	Device damage is expected due to internal current flow.	A
CS-	19	Device damage is expected due to internal current flow.	A
CS+	20	Device damage is expected due to internal current flow.	A
VS	22	Device does not power up.	B
CAP	23	Device is damaged due to internal conduction between VS and CAP.	A
C	24	Linear regulation and reverse current blocking functionality is not available. Device quiescent current can increase.	B
RTN	—	Input reverse polarity protection feature is not available.	B

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Table 4-3. Pin FMA for Device Pins Open Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	Ideal diode FET can not be controlled. Reverse current blocking feature is not available. Load current flows through body diode of the FET.	B
A	2	Ideal diode FET is turned off due to linear regulation sink current. Load current flows through body diode of the FET.	B
SW	3	Battery voltage monitoring feature is not available.	B
UVLO	4	Device HGATE drive is off due to internal pull down on UVLO pin.	B
OV	5	Overvoltage protection functionality is disabled as OV pin is internally pulled low.	B
EN	6	Device is in shutdown mode as EN pin is internally pulled low.	B
SLEEP	7	SLEEP mode feature is not available.	B
N.C	8, 17, 21	No effect on device operation.	D
TMR	9	Device operation with default timer operation. Auto retry timer can not be set using external timer capacitor.	B
IMON	10	Current monitoring output is not available.	B
ILIM	11	ILIM pin is pulled high and device is in overcurrent protection mode.	B
FLT	12	Fault indication functionality is not available.	B
GND	13	Device does not power up.	D
HGATE	14	HGATE control to turn on/off external FET is not available.	B
OUT	15	HGATE control to turn on/off external FET is not available.	D
SLEEP_OV	16	Overvoltage protection during SLEEP mode is not available.	B
ISCP	18	Short circuit protection feature is not available.	B
CS-	19	Device is in overcurrent protection mode and HGATE drive is turned off.	B
CS+	20	Overcurrent protection and current monitoring output is not available.	B
VS	22	Device does not power up.	B
CAP	23	Charge pump does not build up and gate drives DGATE and HGATE are disabled.	B
C	24	DGATE drive remains off.	B
RTN	—	No effect on device operation.	D

Table 4-4. Pin FMA for Device Pins Short Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	Ideal diode FET is off. Load current flows through body diode of the FET.	B
A	2	No effect on device operation.	D
SW	3	UVLO feature is not available.	B
UVLO	4	Either OV or UVLO comparator trigger and HGATE is off.	B
OV	5	HGATE drive is off in case device is enabled (EN=High).	B
EN	6	No effect on device operation.	D
SLEEP	7	No effect on device operation.	D
N.C	8, 17, 21	No effect on device operation.	D
TMR	9	Timer (TMR) and current monitoring (IMON) functionality are out of data sheet specification.	B
IMON	10	Current monitoring output is out of data sheet specification.	B
ILIM	11	Device is in overcurrent protection mode based on \overline{FLT} voltage level.	B
\overline{FLT}	12	No effect on device operation.	D
GND	13	GND shorted to HGATE can cause device damage.	A
HGATE	14	HGATE FET is off as HGATE is shorted to OUT causing VGS short condition.	B
OUT	15	No effect on device operation. Device supports only overvoltage clamp operation during SLEEP mode.	B
SLEEP_OV	16	No effect on device operation.	B
ISCP	18	No effect on device operation.	D
CS-	19	Short circuit and overcurrent protection is not available.	B
CS+	20	Overcurrent limit, current monitoring output parameters are out of specification.	B
VS	22	Device charge pump does not come up. DGATE and HGATE drive are off.	B
CAP	23	Device charge pump does not come up. DGATE and HGATE drive are off.	B
C	24	No effect on device operation.	B
RTN	—	No effect on device operation.	D

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Table 4-5. Pin FMA for Device Pins Short Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	DGATE is shorted to supply. Ideal diode FET remains off.	B
A	2	No effect on device operation.	D
SW	3	Battery voltage monitoring feature is available irrespective of EN pin status.	B
UVLO	4	UVLO functionality is not available.	B
OV	5	HGATE is turned off due to OV comparator input going high.	B
EN	6	Device is always on as EN is pulled to supply.	B
SLEEP	7	SLEEP mode feature is not available.	B
N.C	8, 17, 21	No effect on device operation.	D
TMR	9	Device is damaged if supply voltage level >5.5V.	A
IMON	10	Device is damaged if supply voltage level >5.5V.	A
ILIM	11	Device is damaged if supply voltage level >5.5V.	A
FLT	12	Fault indication functionality is not available.	B
GND	13	Device does not power up due to supply shorted to GND.	D
HGATE	14	HGATE control to turn on/off external FET is not available. Device quiescent current can increase.	B
OUT	15	Supply is shorted to output. Ideal diode (DGATE), load disconnect (HGATE) features will not be functional as supply is shorted to output.	B
SLEEP_OV	16	Device is able to provide overvoltage cut-off functionality only during SLEEP mode.	B
ISCP	18	Device has default short circuit protection threshold of 20mV.	B
CS-	19	Overcurrent protection functionality is not available.	B
CS+	20	Device is in overcurrent protection mode.	B
VS	22	No effect on device operation.	B
CAP	23	Charge pump does not build up and gate drives DGATE and HGATE are disabled.	B
C	24	Ideal diode functionality is not available (reverse current blocking).	B
RTN	—	No effect on device operation.	D

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