Functional Safety Information

TLVM13610 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TLVM13610 (QFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

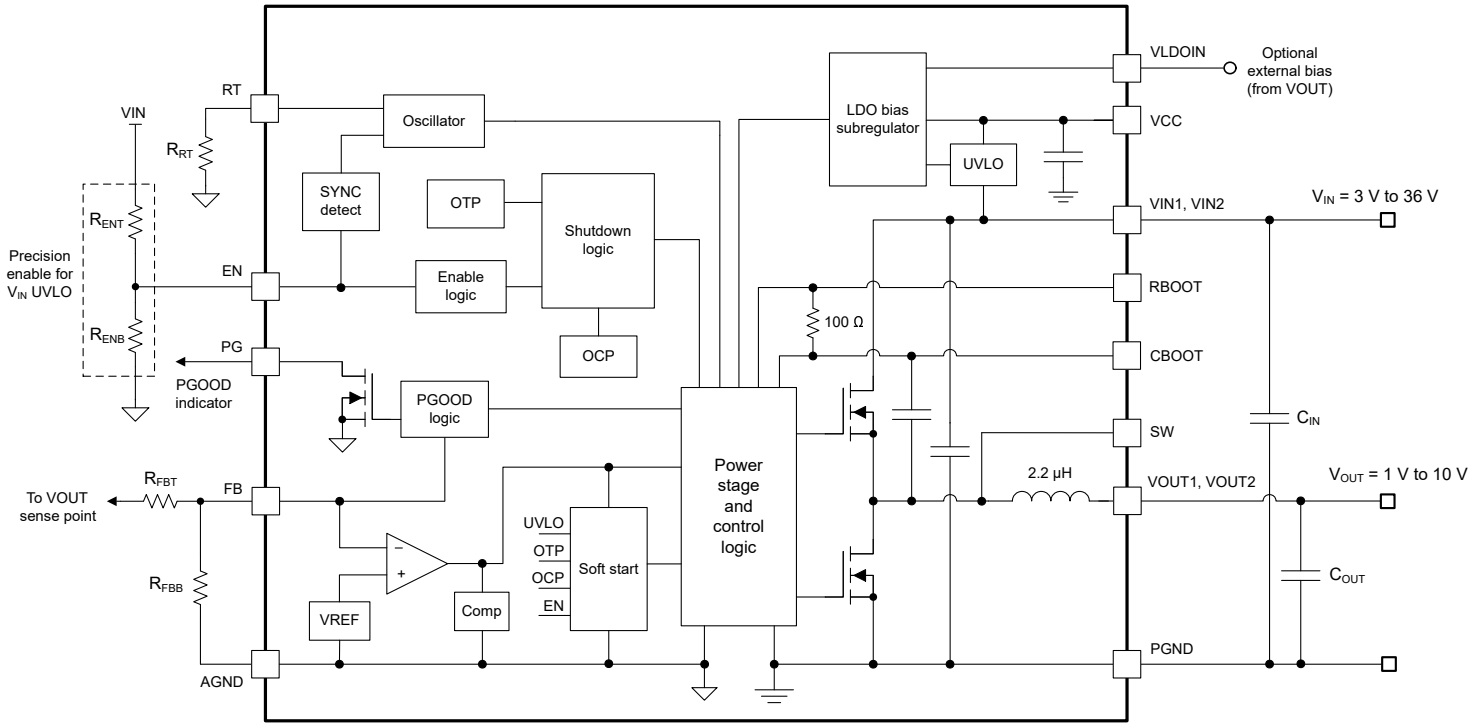

Figure 1-1. Functional Block Diagram

TLVM13610 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLVM13610 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	28
Die FIT Rate	6
Package FIT Rate	22

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed = < 50-V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLVM13610 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60%
Output not in specification — voltage or timing	25%
Gate driver stuck on	5%
Power Good — false trip or fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLVM13610. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TLVM13610 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLVM13610 data sheet.

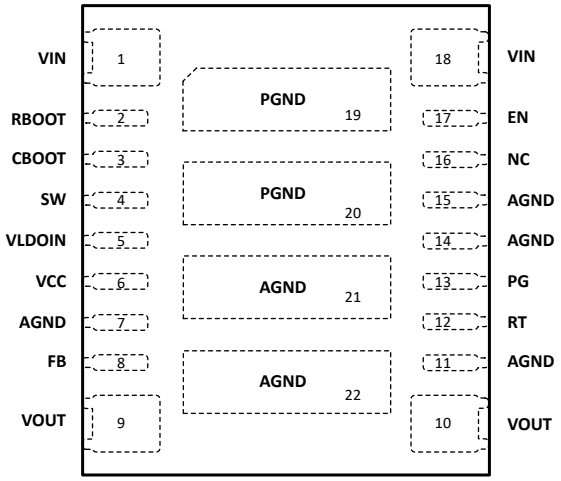

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the TLVM13610 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 18	VOUT = 0 V. Possible damage to customer input supply, PCB can occur unless customer provides protection, or both. Reverse current from the VOUT pin to VIN pin, due to discharge of output capacitors, can damage the regulator.	B
RBOOT	2	Loss of output voltage	A
BOOT	3	Driver supply to high-side MOSFET is lost. Output voltage is regulated. Possible damage to the internal regulator and CBOOT charging circuit	B
SW	4	Shorting the SW pin to ground results in large currents through the device and subsequent damage. No output voltage is produced.	A
VLDOIN	5	Normal operation, IC powers from VIN, causing decreased efficiency.	C
VCC	6	Internal circuits are disabled. No output voltage is generated. Possible increase in input current.	B
AGND	7, 11	No effect	D
FB	8	The regulator operates at maximum duty cycle. Output voltage rised to nearly the input voltage level. Possible damage to customer load, output stage components can occur, or both.	B
VOUT	9, 10	Loss of output voltage	B
RT	12	Switching frequency set to internal 2.2 MHz	C
PG	13	This is a valid connection for the PG output. PG functionality is lost.	D
AGND	14	This is a valid connection for AGND.	D
AGND	15	This is a valid connection for AGND.	D
NC	16	No effect	D
EN	17	This is a valid connection for the EN input. Enable functionality is lost; the device remains off with no output voltage generated.	B
PGND	19, 20, 21, 22	This is the recommended connection for PGND	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1,18	VOUT = 0 V.	B
RBOOT	2	Normal operation. Device uses internal 100 Ω for slowest switch-node slew rate.	D
BOOT	3	Normal operation. Device uses internal 100-nF bootstrap capacitor.	D
SW	4	Normal operation	D
VLDOIN	5	Normal operation, IC powers from VIN, causing decreased efficiency	C
VCC	6	Normal operation	D
AGND	7, 11	Load regulation degraded	C
FB	8	VOUT >> than programmed output voltage	B
VOUT	9,10	Loss of output regulation	B
RT	12	Loss of output regulation	C
PG	13	This is a valid connection for the PG output. PG functionality is lost.	D
AGND	14	May have output voltage ripple increase	C
AGND	15	Mode may switch randomly. Unpredictable behavior	C
NC	16	Valid connection	D
EN	17	Loss of enable functionality. Erratic operation; probable loss of regulation.	B
PGND	19, 20, 21, 22	Load regulation degraded, thermal impedance impacted. Loss of operation if all four pins are open.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Shorted To	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	RBOOT	VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND	A
RBOOT	2	BOOT	VOUT normal operation	D
BOOT	3	SW	Loss of output regulation	B
SW	4	VLDOIN	If SW > 20 V, damage to VLDOIN pin	A
VLDOIN	5	VCC	If VLDO > 5 V, damage to VCC pin	A
VCC	6	AGND	Internal circuit disabled	B
AGND	7	FB	VOUT >> than programmed output voltage, regulate close to VIN	B
FB	8	VOUT	VOUT << than programmed output voltage, regulate to reference voltage	B
VOUT	9	VOUT	Valid connection	D
VOUT	10	AGND	Loss of output regulation	C
AGND	11	RT	Switching frequency set to 2.1MHz	C
RT	12	PG	If PG low, switching frequency set to 2.1 MHz. If PG high, switching frequency is set to 400 kHz.	C
PG	13	SPSP	PG low at start-up, spread spectrum is disabled.	C
AGND	14	AGND	Normal operation	D
AGND	15	NC	Normal operation	D
NC	16	EN	EN pin left floating. Loss of enable functionality. Erratic operation; probably loss of regulation.	B
EN	17	VIN	Loss of precision enable feature. Device operates normally.	D
VIN	18	VIN	Valid connection	D
PGND	19, 20, 21, 22	Any	Other pin is shorted to ground, see Table 4-2	—

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 18	No effect	D
RBOOT	2	VOUT = 0 V. RBOOT ESD clamp runs current to destruction.	A
BOOT	3	VOUT = 0 V. BOOT ESD clamp runs current to destruction.	A
SW	4	Damage to low-side FET	A
VLDOIN	5	If VIN exceeds 16 V, damage occurs. If below 16 V, normal operation.	A
VCC	6	If VIN exceeds 5.5 V damage occurs.	A
AGND	7, 11	VOUT = 0 V. Damage to other pins referred to GND.	A
FB	8	If VIN exceeds 5.5 V, damage occurs. VOUT = 0 V.	A
VOUT	9, 10	Damage to low-side FET. The output voltage rises to nearly the level of VIN. Customer load is damaged. Possible damage to device.	A
RT	12	VOUT = 0 V	B
PG	13	VOUT = 0 V. PGOOD ESD clamp runs current to destruction.	A
AGND	14	May have output voltage ripple increase	D
AGND	15	Efficiency decrease in light-load	C
NC	16	No effect	D
EN	17	Loss of precision enable feature. Device operates normally.	D
PGND	19, 20, 21, 22	VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265