Functional Safety Information

DP83TC814 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for DP83TC814 to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

DP83TC814 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for DP83TC814 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	25
Die FIT rate	3
Package FIT rate	22

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 290 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DP83TC814 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Fault in MDI transmitter causing IEEE spec compliance issues	8
Fault in MDI transmitter causing high RF emissions	4
Fault in MDI receiver causing poor-link quality/link-loss	8
Fault in internal power circuits causing poor link quality and higher power consumption	12
Fault in internal clock circuits causing IEEE compliance issues and poor link-quality	8
Fault in GPIO causing higher RF emissions	8
Fault in GPIO causing Rgmii/JEDEC/Datasheet spec violation	8
Fault in ESD on MDI making IEC ESD performance lower than 8KV	4
Fault in ESD on GPIOs making CDM performance lower than 2KV.	4
Digital core has stuck or transient faults causing link-up or PCS faults	36

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of DP83TC814. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (seeTable 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5, Table 4-6, and Table 4-7).

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DP83TC814 data sheet.

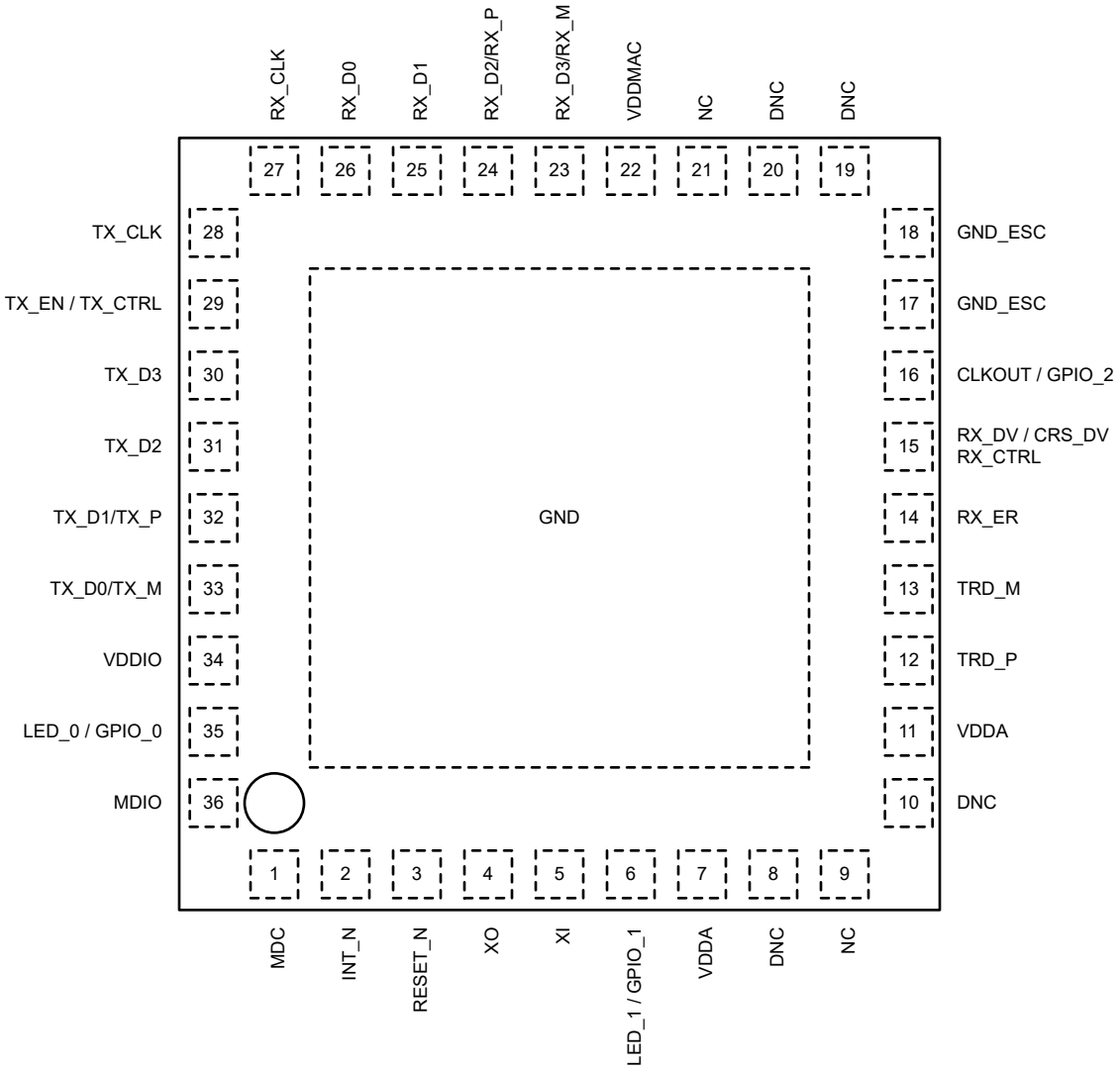

Figure 4-1. DP83TC814S-Q1 RHA Package 36-Pin VQFN

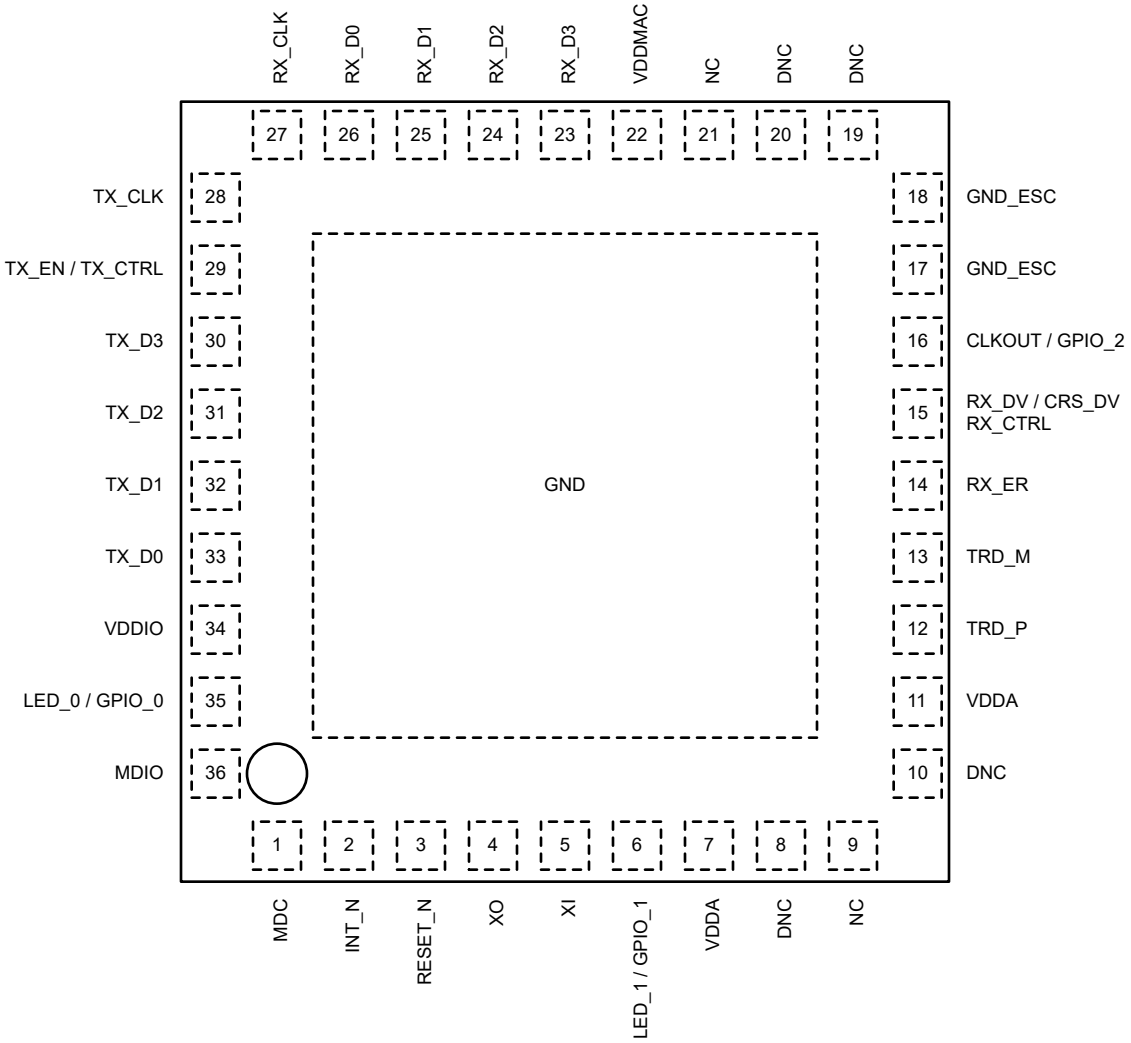

Figure 4-2. DP83TC814R-Q1 RHA Package 36-Pin VQFN

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MDC	1	No SMI communication available	B
INT	2	No valid interrupt status	B
RESET	3	Device in Reset state	B
XO	4	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known	B
XI	5	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known	B
LED_1	6	GPIO_1 not operational	B
VDDA	7	Device is disabled. Core supply short	B
DNC	8	No issue	D
NC	9	No issue	D
DNC	10	No issue	D
VDDA	11	Device is disabled. Core supply short	B
TRD_P	12	Link/data transfer cannot occur	A
TRD_M	13	Link/data transfer cannot occur	A
RX_ER	14	Valid data cannot be sent to MAC	B
RX_CTRL	15	Valid data cannot be sent to MAC	B
CLKOUT	16	GPIO_2 not operational. Daisy chaining won't work if CLKOUT used to give clock to another PHY	B
GND_ESC	17	No issue	D
GND_ESC	18	No issue	D
DNC	19	No issue	D
DNC	20	No issue	D
NC	21	No issue	D
VDDMAC	22	MAC supply short	B
RX_D3	23	Valid data cannot be sent to MAC	B
RX_D2	24	Valid data cannot be sent to MAC	B
RX_D1	25	Valid data cannot be sent to MAC	B
RX_D0	26	Valid data cannot be sent to MAC	B
RX_CLK	27	Valid data cannot be sent to MAC	B
TX_CLK	28	Valid data cannot be received	B
TX_CTRL	29	Valid data cannot be received	B
TX_D3	30	Valid data cannot be received	B
TX_D2	31	Valid data cannot be received	B
TX_D1	32	Valid data cannot be received	B
TX_D0	33	Valid data cannot be received	B
VDDIO	34	IO supply short	B
LED_0	35	GPIO_0 not operational, link-up can still happen with register write for master	B
MDIO	36	No SMI communication available	B
DAP	GND	Appropriate connection	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MDC	1	No SMI communication available	B
INT	2	Interrupt will not be available	B
RESET	3	Normal Operation	D
XO	4	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known	B
XI	5	Crystal resonator clock will not start-up. Device PLL not operational. PHY state not known	B
LED_1	6	Normal Operation	D
VDDA	7	Device is disabled. Core supply open	B
DNC	8	No issue	D
NC	9	No issue	D
DNC	10	No issue	D
VDDA	11	Device is disabled. Core supply open	B
TRD_P	12	Link/data transfer cannot occur	B
TRD_M	13	Link/data transfer cannot occur	B
RX_ER	14	Valid data cannot be sent to MAC	B
RX_CTRL	15	Valid data cannot be sent to MAC	B
CLKOUT	16	No issue	D
GND_ESC	17	No issue	D
GND_ESC	18	No issue	D
DNC	19	No issue	D
DNC	20	No issue	D
NC	21	No issue	D
VDDMAC	22	Device is disabled. MAC supply open	B
RX_D3	23	Valid data cannot be sent to MAC	B
RX_D2	24	Valid data cannot be sent to MAC	B
RX_D1	25	Valid data cannot be sent to MAC	B
RX_D0	26	Valid data cannot be sent to MAC	B
RX_CLK	27	Valid data cannot be sent to MAC	B
TX_CLK	28	Valid data cannot be received	B
TX_CTRL	29	Valid data cannot be received	B
TX_D3	30	Valid data cannot be received	B
TX_D2	31	Valid data cannot be received	B
TX_D1	32	Valid data cannot be received	B
TX_D0	33	Valid data cannot be received	B
VDDIO	34	Device is disabled. IO supply open	B
LED_0	35	Link-up can still happen with register write for master	B
MDIO	36	No SMI communication available	B
DAP	GND	Ground open	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
MDC	1	INT	No SMI communication available, No valid interrupt status	B
INT	2	RESET	When device intending to give interrupt it enters reset. Also, when host resets the PHY, host will get ISR triggered	B
RESET	3	XO	Device will keep getting reset	B
XO	4	XI	Device in unknown state	B
XI	5	LED_1	Device in unknown state	B
LED_1	6	VDDA	Device may get damaged.	A
VDDA	7	DNC	Device may get damaged	A
DNC	8	NC	No issue	D
NC	9	DNC	No issue	D
DNC	10	VDDA	Device may get damaged	A
VDDA	11	TRD_P	Link/data transfer cannot occur	A
TRD_P	12	TRD_M	Link/data transfer cannot occur	B
TRD_M	13	RX_ER	Link/data transfer cannot occur	B
RX_ER	14	RX_CTRL	Communication to MAC may be lost. Valid data will trigger an error	B
RX_CTRL	15	CLKOUT	Spurious data transfer. CLKOUT may have glitches	B
CLKOUT	16	GND_ESC	No issue	D
GND_ESC	17	GND_ESC	No issue	D
GND_ESC	18	DNC	No issue	D
DNC	19	DNC	No issue	D
DNC	20	NC	No issue	D
NC	21	VDDMAC	No issue	D
VDDMAC	22	RX_D3	Valid data cannot be sent to MAC	B
RX_D3	23	RX_D2	Valid data cannot be sent to MAC	B
RX_D2	24	RX_D1	MAC interface selection may be corrupt. Valid data cannot be sent to MAC	B
RX_D1	25	RX_D0	MAC interface selection may be corrupt. Valid data cannot be sent to MAC	B
RX_D0	26	RX_CLK	MAC interface selection may be corrupt. Valid data cannot be sent to MAC	B
RX_CLK	27	TX_CLK	Valid data cannot be exchanged with MAC	B
TX_CLK	28	TX_CTRL	Valid data cannot be received	B
TX_CTRL	29	TX_D3	Valid data cannot be received	B
TX_D3	30	TX_D2	Valid data cannot be received	B
TX_D2	31	TX_D1	Valid data cannot be received	B
TX_D1	32	TX_D0	Valid data cannot be received	B
TX_D0	33	VDDIO	Valid data cannot be received	B
VDDIO	34	LED_0	Valid data cannot be received. Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
LED_0	35	MDIO	Link-up still possible through register write. Spurious LED glow/blink	B
MDIO	36	MDC	No SMI communication available.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDDIO

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MDC	1	No SMI communication available	B
INT	2	No interrupt status	B
RESET	3	Can never reset the device	B
XO	4	PHY state not known	B
XI	5	PHY state not known	B
LED_1	6	GPIO not operational, Device will enter standby mode. Need register write to start link-up	B
VDDA	7	Device may not power up	B
DNC	8	Device may get damaged	A
NC	9	No issue	D
DNC	10	Device may get damaged	A
VDDA	11	Device may not power up	B
TRD_P	12	Link/data transfer cannot occur. Device may get damaged	A
TRD_M	13	Link/data transfer cannot occur. Device may get damaged	A
RX_ER	14	PHY Address range restricted. MDC/MDIO communication could be lost. Device may get damaged when VDDIO and VDDMAC are different	B
RX_CTRL	15	PHY Address range restricted. MDC/MDIO communication could be lost. Device may get damaged when VDDIO and VDDMAC are different	B
CLKOUT	16	GPIO not operational. Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
GND_ESC	17	No issue	D
GND_ESC	18	No issue	D
DNC	19	Device may get damaged	A
DNC	20	Device may get damaged	A
NC	21	No issue	D
VDDMAC	22	No issue	D
RX_D3	23	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
RX_D2	24	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
RX_D1	25	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
RX_D0	26	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
RX_CLK	27	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
TX_CLK	28	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
TX_CTRL	29	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
TX_D3	30	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
TX_D2	31	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
TX_D1	32	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
TX_D0	33	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
VDDIO	34	Appropriate connection	D
LED_0	35	GPIO_0 not operational. Device will be always in master mode. May need register write for linkup	B
MDIO	36	No SMI communication available	B
DAP	GND	Device may get damaged	A

Table 4-6. Pin FMA for Device Pins Short-Circuited to VDDMAC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MDC	1	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
INT	2	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
RESET	3	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
XO	4	PHY state not known	B
XI	5	PHY state not known	B
LED_1	6	Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
VDDA	7	Device may not power up	B
DNC	8	Device may get damaged	A
NC	9	No issue	D
DNC	10	Device may get damaged	A
VDDA	11	Device may not power up	B
TRD_P	12	Link/data transfer cannot occur. Device may get damaged	A
TRD_M	13	Link/data transfer cannot occur. Device may get damaged	A
RX_ER	14	PHY Address range restricted. MDC/MDIO communication could be lost. Invalid data triggered to the MAC	B
RX_CTRL	15	PHY Address range restricted. MDC/MDIO communication could be lost. Invalid data triggered to the MAC	B
CLKOUT	16	GPIO not operational.	B
GND_ESC	17	No issue	D
GND_ESC	18	No issue	D
DNC	19	Device may get damaged	A
DNC	20	Device may get damaged	A
NC	21	No issue	D
VDDMAC	22	No issue	D
RX_D3	23	Valid data cannot be sent to MAC	B
RX_D2	24	Valid data cannot be sent to MAC	B
RX_D1	25	Valid data cannot be sent to MAC	B
RX_D0	26	Valid data cannot be sent to MAC	B
RX_CLK	27	Valid data cannot be sent to MAC	B
TX_CLK	28	Valid data cannot be received from MAC	B
TX_CTRL	29	Valid data cannot be received from MAC	B
TX_D3	30	Valid data cannot be received from MAC	B
TX_D2	31	Valid data cannot be received from MAC	B
TX_D1	32	Valid data cannot be received from MAC	B
TX_D0	33	Valid data cannot be received from MAC	B
VDDIO	34	Device will be functional	D
LED_0	35	GPIO_0 not operational. Device will be always in master mode. May need register write for linkup. Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
MDIO	36	No SMI communication available. Device may get damaged when VDDIO and VDDMAC are of different voltage levels	A
DAP	GND	Device may get damaged	A

Table 4-7. Pin FMA for Device Pins Short-Circuited to VDDA

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MDC	1	Device may get damaged	A
INT	2	Device may get damaged	A
RESET	3	Device may get damaged	A
XO	4	PHY state not known	B
XI	5	PHY state not known	B
LED_1	6	Device may get damaged	A
VDDA	7	Appropriate connection	D
DNC	8	Device may get damaged	A
NC	9	No issue	D
DNC	10	Device may get damaged	A
VDDA	11	Appropriate connection	D
TRD_P	12	Link/data transfer cannot occur. Device may get damaged	A
TRD_M	13	Link/data transfer cannot occur. Device may get damaged	A
RX_ER	14	Device may get damaged	A
RX_CTRL	15	Device may get damaged	A
CLKOUT	16	Device may get damaged	A
GND_ESC	17	No issue	D
GND_ESC	18	No issue	D
DNC	19	Device may get damaged	A
DNC	20	Device may get damaged	A
NC	21	No issue	D
VDDMAC	22	Device will be functional	D
RX_D3	23	Device may get damaged	A
RX_D2	24	Device may get damaged	A
RX_D1	25	Device may get damaged	A
RX_D0	26	Device may get damaged	A
RX_CLK	27	Device may get damaged	A
TX_CLK	28	Device may get damaged	A
TX_CTRL	29	Device may get damaged	A
TX_D3	30	Device may get damaged	A
TX_D2	31	Device may get damaged	A
TX_D1	32	Device may get damaged	A
TX_D0	33	Device may get damaged	A
VDDIO	34	Device will be functional	D
LED_0	35	Device may get damaged	A
MDIO	36	No SMI communication available. Device may get damaged	A
DAP	GND	Device may get damaged	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Initial Release

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