

OPAx607-Q1

Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	3
2.1 DBV Package.....	3
2.2 DGK Package.....	4
3 Failure Mode Distribution (FMD)	5
4 Pin Failure Mode Analysis (Pin FMA)	6
4.1 DBV Package.....	7
4.2 DGK Package.....	8

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for the OPAx607-Q1 (DBV and DGK packages) to aid in a functional safety system design. The DBV package corresponds to the single-channel amplifier, while the DGK package corresponds to the dual-channel amplifier. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

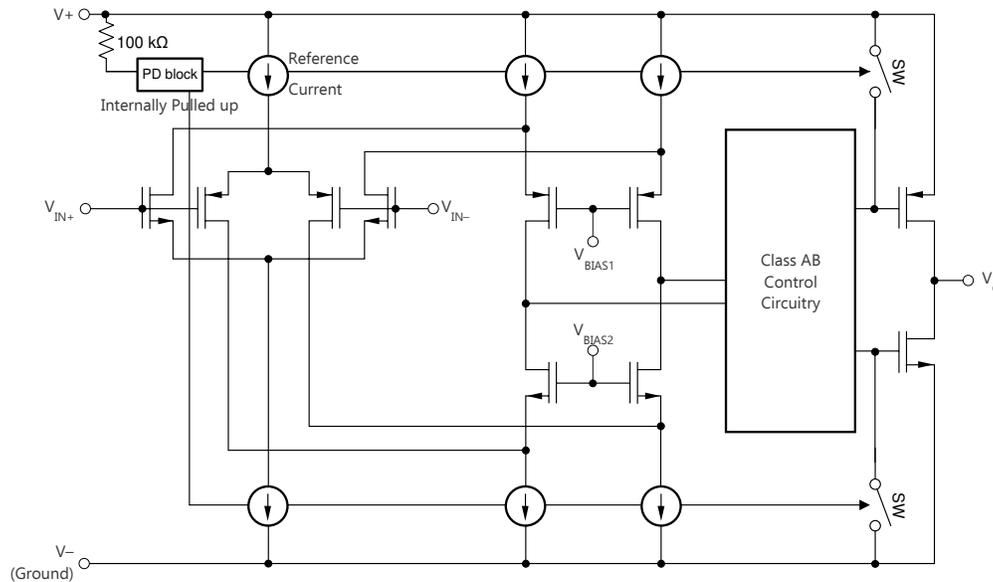


Figure 1-1. Functional Block Diagram

The OPAx607-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DBV Package

This section provides functional safety failure in time (FIT) rates for the DBV package of the OPAx607-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 5.75 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
4	BICMOS Op Amp, Comparators, Voltage Monitors	4 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DGK Package

This section provides functional safety failure in time (FIT) rates for the DGK package of the OPax607-Q1 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	5
Die FIT rate	2
Package FIT rate	3

The failure rate and mission profile information in [Table 2-3](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 11.5 mW
- Climate type: World-wide table 8
- Package factor (λ_3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
4	BICMOS Op Amp, Comparators, Voltage Monitors	4 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the OPAx607-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output is floating, open	20
Output is stuck, high	20
Output is stuck, low	20
Output functional, not in specification	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the OPAX607-Q1 (DBV and DGK packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#) and [Table 4-6](#))
- Pin open-circuited (see [Table 4-3](#) and [Table 4-7](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#) and [Table 4-8](#))
- Pin short-circuited to supply (see [Table 4-5](#) and [Table 4-9](#))

[Table 4-2](#) through [Table 4-9](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is running in the typical configuration and application, as seen in the *Normal Operating Mode* section in the OPAX607-Q1 data sheet.
- Total supply voltage of 5V with V_{S+} connected to 5V and V_{S-} connected to 0V (GND).
- Input and output pins biased to a 2.5V reference point
- Device is configured with feedback network in gain greater than or equal to 1V/V

4.1 DBV Package

Figure 4-1 shows the OPAx607-Q1 pin diagram for the DBV package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the OPAx607-Q1 data sheet.

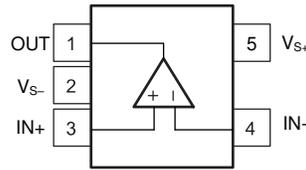


Figure 4-1. Pin Diagram (DBV) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Short to GND may cause device to overheat.	B
VS-	2	Normal operation if single supply configuration is used.	D
IN+	3	Input at VS- (GND) is valid input, however, desired application result is unlikely.	C
IN-	4	Input at VS- (GND) is valid input, however, desired application result is unlikely.	C
VS+	5	Diodes from input to VS+ may turn on due to input signal and cause electrical overstress (EOS).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the device, but the output will not be measured.	C
VS-	2	Lowest voltage output pin will try to power the VS- pin of the device.	B
IN+	3	Floating input, circuit will likely not function as expected.	C
IN-	4	Floating input, circuit will likely not function as expected.	C
VS+	5	Highest voltage output pin will try to power the VS+ pin of the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	VS-	Short to VS- may cause device to overheat.	B
VS-	2	IN+	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
IN+	3	IN-	No damage to device. Application circuit will not work. Pins are not adjacent to each other.	C
IN-	4	VS+	May cause device to overheat. Input at VS+ is not a valid input. Pins are not as near to each other, due to package type.	B
VS+	5	OUT	Short to VS+ may cause device to overheat. Pins are not adjacent to each other.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Short to VS+ may cause device to overheat.	B
VS-	2	Diodes from input to VS- may turn on due to input signal and cause electrical overstress (EOS).	A
IN+	3	Input at VS+ is a valid input, however, desired application result is unlikely.	C
IN-	4	Input at VS+ is a valid input, however, desired application result is unlikely.	C
VS+	5	Normal operation.	D

4.2 DGK Package

Figure 4-2 shows the OPAx607-Q1 pin diagram for the DGK package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the OPAx607-Q1 data sheet.

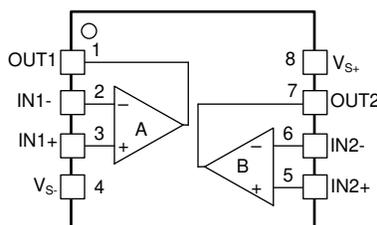


Figure 4-2. Pin Diagram (DGK Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT1	1	Short to GND may cause device to overheat.	B
IN1-	2	Input at V_{S-} (GND) is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V_{S-} (GND) is valid input, however, desired application result is unlikely.	C
V_{S-}	4	Normal Operation if single supply configuration is used.	D
OUT2	5	May cause device to overheat.	B
IN2+	6	Input at V_{S-} (GND) is valid input, however, desired application result is unlikely.	C
IN2-	7	Input at V_{S-} (GND) is valid input, however, desired application result is unlikely.	C
V_{S+}	8	Diodes from input to V_{S+} may turn on due to input signal and cause electrical overstress (EOS).	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT1	1	Output can be left open. There is no effect on the device, but the output will not be measured.	C
IN1-	2	Floating input; circuit will likely not function as expected.	C
IN1+	3	Floating input; circuit will likely not function as expected.	C
V_{S-}	4	Lowest voltage output pin will try to power the V_{S-} pin of the device.	B
OUT2	5	Output can be left open. There is no effect on the device, but the output will not be measured.	C
IN2+	6	Floating input; circuit will likely not function as expected.	C
IN2-	7	Floating input; circuit will likely not function as expected.	C
V_{S+}	8	Highest voltage output pin will try to power the V_{S+} pin of the device.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT1	1	IN1-	Channel 1 configured in unity gain.	C
IN1-	2	IN1+	No damage to device. Application circuit will not work.	C
IN1+	3	V_{S-}	Input at V_{-} (GND) is valid input, however, desired application result is unlikely.	C
V_{S-}	4	IN2+	Input at V_{-} (GND) is valid input, however, desired application result is unlikely. Pins are not adjacent to each other.	C
IN2+	5	IN2-	No damage to device. Application circuit will not work.	C
IN2-	6	OUT2	Channel 2 configured in unity gain	C
OUT2	7	V_{S+}	Short to V_{S+} may cause device to overheat.	B
V_{S+}	8	OUT1	Short to V_{S+} may cause device to overheat. Pins are not adjacent to each other.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT1	1	Short to V_{S+} may cause device to overheat.	B
IN1-	2	Input at V_{S+} (GND) is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V_{S+} (GND) is valid input, however, desired application result is unlikely.	C
V_{S-}	4	Diodes from input to V_{S-} may turn on due to input signal and cause electrical overstress (EOS).	A
OUT2	5	Short to V_{S+} may cause device to overheat.	B
IN2+	6	Input at V_{S+} (GND) is valid input, however, desired application result is unlikely.	C
IN2-	7	Input at V_{S+} (GND) is valid input, however, desired application result is unlikely.	C
V_{S+}	8	Normal operation.	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated