Functional Safety Information

TPSM33625 and TPSM33615 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPSM33625 and TPSM33615 (QFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

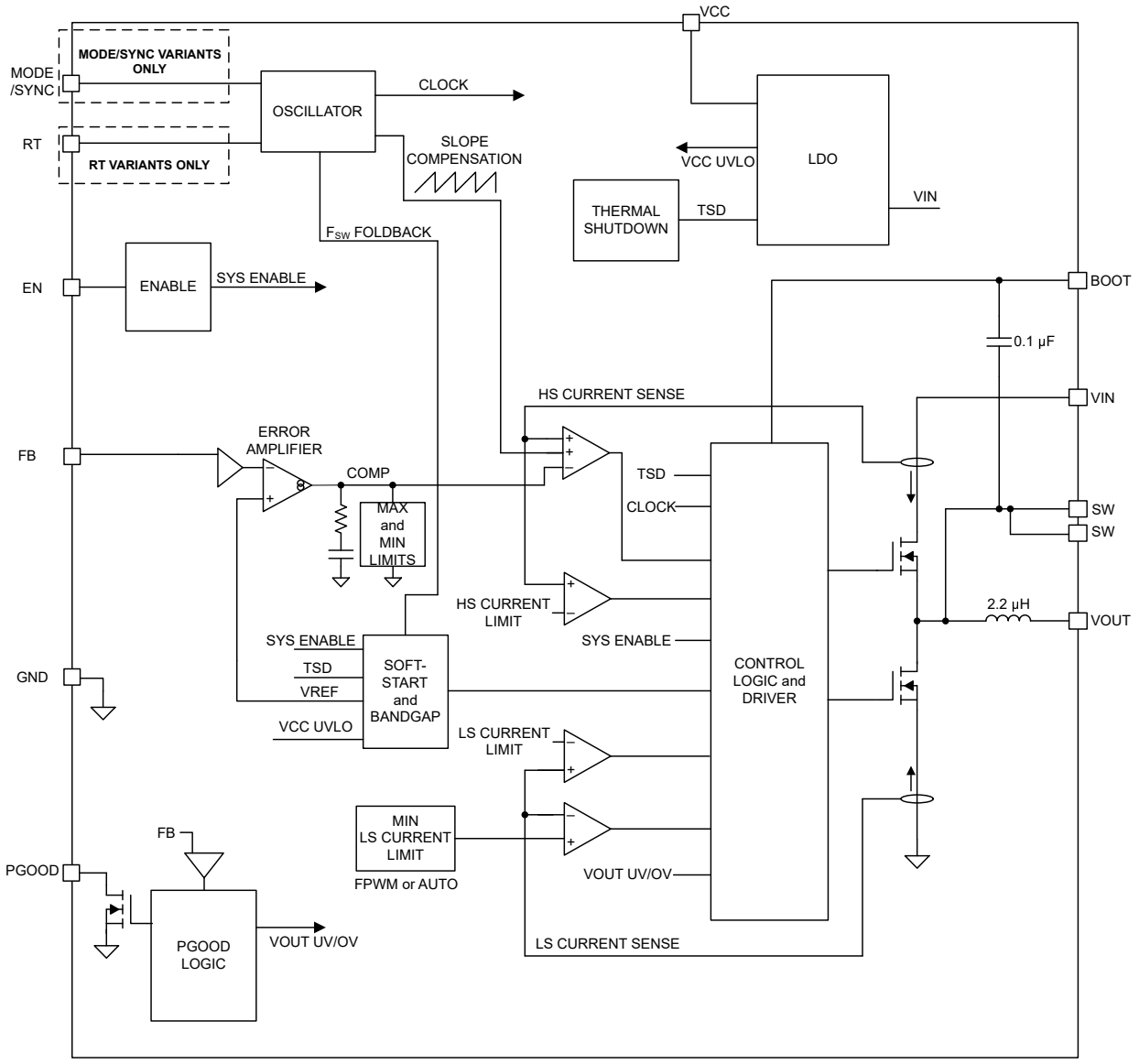

Figure 1-1. Functional Block Diagram

The TPSM33625 and TPSM33615 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPSM33625 and TPSM33615 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	30
Die FIT rate	6
Package FIT rate	24

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog and mixed = <50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPSM33625 and TPSM33615 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60
Output not in specification–voltage or timing	30
PG false trip or fails to trip	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPSM33625 and TPSM33615. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPSM33625 and TPSM33615 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPSM33625 and TPSM33615 data sheets.

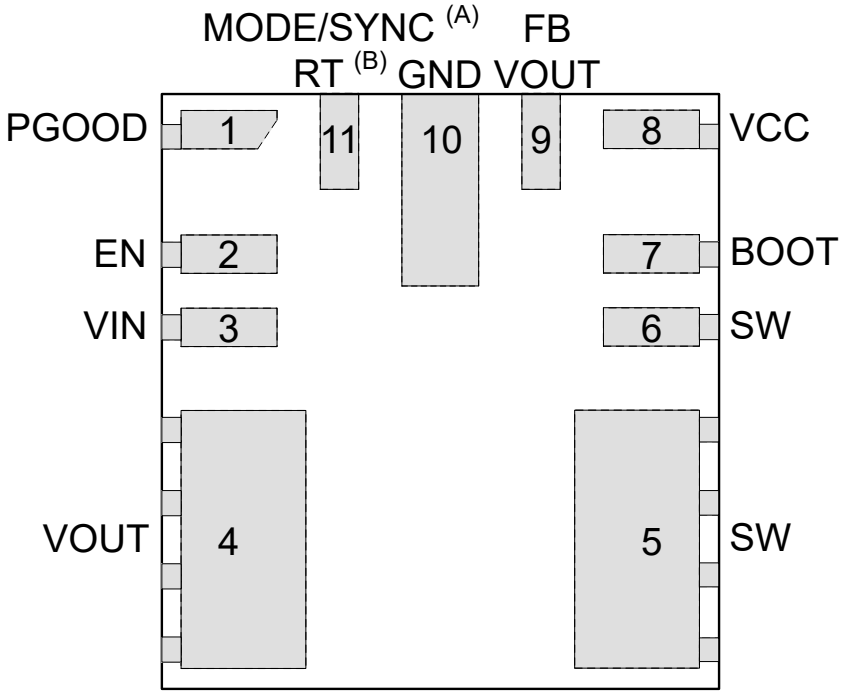

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The product data sheet application circuit is followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PGOOD	1	When not in use, this pin can be left grounded (PGOOD is not a valid signal and VOUT is normal).	D
EN/UVLO	2	VOUT = 0V; part is disabled.	B
VIN	3	VOUT = 0V.	B
VOUT	4	Goes into hiccup; short-circuit operation.	B
SW	5	Device damage.	A
	6		
BOOT	7	VOUT = 0V, the high-side FET does not turn on.	B
VCC	8	Internal circuits are disabled. No output voltage is generated.	B
FB	9	Switches at maximum duty cycle and VOUT approaches VIN.	B
GND	10	VOUT normal.	D
RT	11	Switching frequency is 2.2MHz.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PGOOD	1	When not in use, this pin can be left open (PGOOD is not a valid signal and VOUT is normal).	D
EN/UVLO	2	Pin cannot be left floating.	B
VIN	3	VOUT = 0V.	B
VOUT	4	Loss of output voltage.	B
SW	5	Normal operation.	D
	6		
BOOT	7	Normal operation.	D
VCC	8	VCC output is unstable, can increase above 5.5V.	A
FB	9	Switches at maximum duty cycle and VOUT approaches VIN. Damage to customer load and output stage components are possible. No effect on device.	B
GND	10	VOUT can be abnormal, as reference voltage is not fixed.	B
RT	11	If part is RT, frequency is not defined. If part is MODE/SYNC, then part can go back and forth between FPWM and PFM. The part is up and functional.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RT	11	PGOOD	If PGOOD is high and < 5.5V, Fsw = 1MHz; if PGOOD is low, Fsw = 2.2MHz. RT or MODE/SYNC absolute maximum is 5.5V.	A
PGOOD	1	EN/UVLO	If EN > 20V, devices connected to the PGOOD pin are damaged.	A
EN/UVLO	2	VIN	VOUT normal.	D
VIN	3	SW	Damage to the low-side FET.	A
SW	5	BOOT	VOUT = 0V, the high-side does not turn on, no CBOOT.	B
	6			
BOOT	7	VCC	Damage occurs, breaks the VCC pin.	A
VCC	8	FB	Can be nonfunctional, no damage occurs.	B
FB	9	GND	Switches at maximum duty cycle and VOUT approaches VIN.	B
GND	10	RT	VOUT is normal if RT/MODE/SYNC pin is low, otherwise not functional.	D
VOUT	4	SW	Damage occurs.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PGOOD	1	If VIN > 20V, damage to PGOOD occurs.	A
EN/UVLO	2	VOUT normal.	D
VIN	3	VOUT normal.	D
VOUT	4	Damage occurs if VIN > 16V. Customer load is damaged.	A
SW	5	Damage to the low-side FET.	A
	6		
BOOT	7	Damage occurs and BOOT ESD clamp is damaged.	A
VCC	8	If VIN > 5.5V, damage occurs.	A
FB	9	Damage occurs if VIN > 16V.	A
GND	10	VOUT = 0V.	B
RT	11	If VIN > 5.5V, damage occurs. If VIN < 5.5V, switching frequency is 1MHz.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 2, 2024 to September 12, 2025 (from Revision A (March 2024) to Revision B (September 2025)) **Page**

- Corrected functional block diagram to remove fixed output configuration....2
- Changed failure description for VOUT pin open-circuited....5
- Changed failure effect class for FB pin open-circuited from C to B....5
- Changed failure effect class for GND pin open-circuited from C to B....5

Changes from September 28, 2022 to March 1, 2024 (from Revision * (September 2022) to Revision A (March 2024)) **Page**

- Added TPSM33615 to document....2

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