Functional Safety Information

LM51231-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LM51231-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

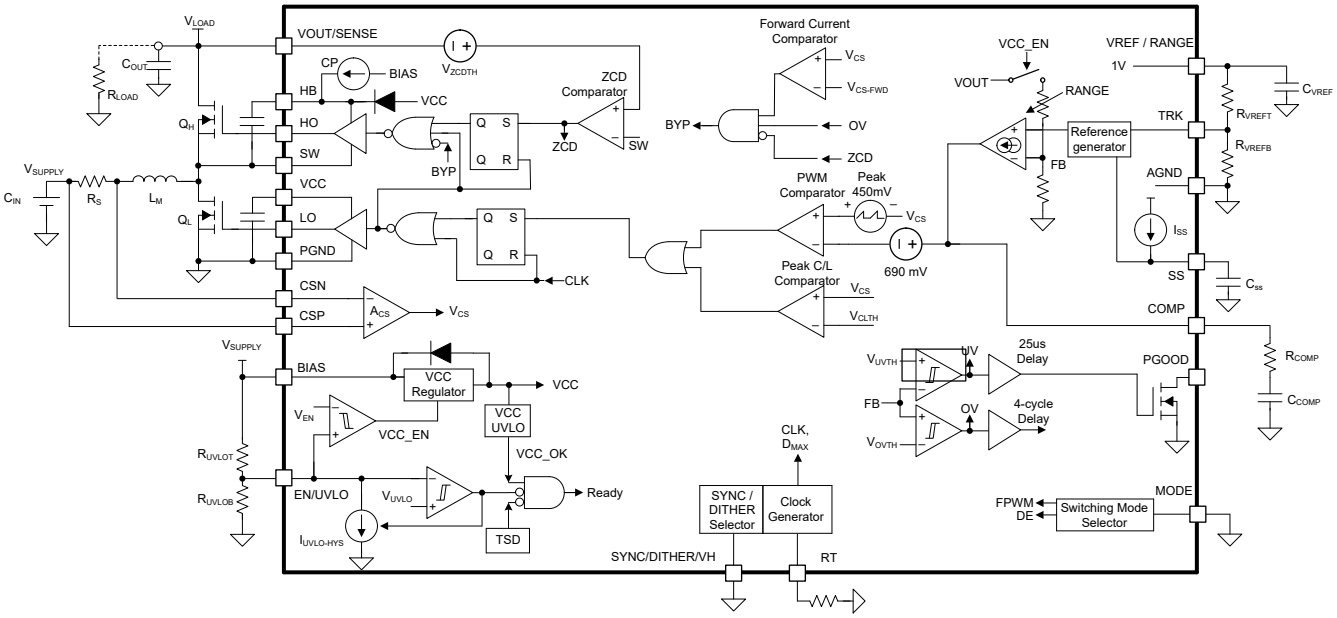

Figure 1-1. Functional Block Diagram

The LM51231-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM51231-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	7
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 800 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog and Mixed HV >50V supply	30 FIT	75ºC

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM51231-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO or LO gate driver stuck on	10
HO or LO gate driver stuck off	20
HO or LO gate driver open (high-Z)	5
VOUT voltage not in specification	30
PGOOD false trip or fails to trip	35

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM51231-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM51231-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM51231-Q1 data sheet.

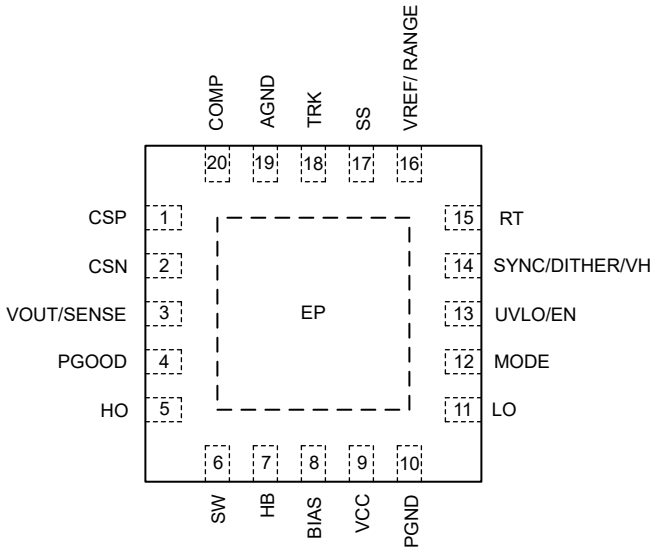

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the LM51231-Q1 data sheet.
- For the analysis, the typical application as shown in the *Typical Application* section of the LM51231-Q1 is used
- V_{SUPPLY} = V_{BIAS} = 12 V
- V_{OUT} = 24 V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CSP	1	CSP Pin can be damaged due to the differential voltage exceeds the 0.3V abs max rating.	A
CSN	2	CSN Pin can be damaged due to the differential voltage exceeds the 0.3V abs max rating.	A
VOUT/SENSE	3	VOUT out of regulation, possible over charge of the output voltage	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PGOOD	4	Correct output voltage, but loss of power-good functionality.	C
HO	5	High-side driver can be damaged when SW voltage rises	A
SW	6	No energy transferred from input to output	B
HB	7	Can be damaged when SW voltage rises	A
BIAS	8	Device unpowered and therefore not functional.	B
VCC	9	Loss of VCC regulation, no switching	B
PGND	10	No effect.	D
LO	11	VOUT out of regulation. LO stops switching.	B
MODE	12	Diode emulation mode is activated. No effect in case the device is configured for diode emulation mode (MODE = GND).	C
UVLO/EN	13	Device is disabled.	B
SYNC/ DITHER/VH	14	External Clock Synchronization is disabled. Spread Spectrum is disabled. VCC is not hold when EN = GND. No effect in case External Clock Synchronization and Spread Spectrum are disabled as well as the VCC hold function is disabled (SYNC/DITHER/VH = GND).	C
RT	15	Maximum switching frequency much greater than 2.21 MHz	C
VREF/RANGE	16	No switching. Target output voltage is 0 V	B
SS	17	Device does not start, no switching	B
TRK	18	VOUT out of regulation, no switching	B
AGND	19	No effect.	D
COMP	20	VOUT out of regulation, not switching.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CSP	1	Loss of current sense signal.	B
CSN	2	Loss of current sense signal.	B
VOUT/SENSE	3	VOUT out of regulation, possible over charge of the output voltage	A
PGOOD	4	Correct output voltage, but loss of power-good functionality.	C
HO	5	Loss of high side driver. Operating with sync FET body diode conducting.	C
SW	6	Loss of high side driver. Operating with sync FET body diode conducting.	C
HB	7	Loss of boot voltage and hence high side driver. Operating with sync FET body diode conducting.	C
BIAS	8	Device unpowered and therefore not functional.	B
VCC	9	No stable VCC to sustain normal operation	B
PGND	10	Possible device damage.	A
LO	11	Low-side MOSFET never switched.	B
MODE	12	No effect if diode emulation mode is active, otherwise diode emulation mode is activated.	C
UVLO/EN	13	Device is disabled.	B
SYNC/ DITHER/VH	14	Loss of VCC hold up functionality	C
RT	15	Minimum frequency is set.	C
VREF/RANGE	16	VOUT out of regulation,	B
SS	17	Small soft-start time. Normal operation after	C
TRK	18	VOUT out of regulation	B
AGND	19	Possible device damage.	A
COMP	20	Device may be unstable.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
CSP	1	CSN	Loss of current sense information. Circuit possibly unstable	C
CSN	2	VOUT/SENSE	Possible damage. Exceeds absolute maximum voltage rating	A
VOUT/SENSE	3	PGOOD	Loss of VOUT feedback. Possibly unstable operation	B
PGOOD	4	HO	No damage, loss of PGOOD function	B
HO	5	SW	Loss of high side driver. Operating with sync FET body diode conducting.	B
SW	6	HB	Loss of boot voltage and hence high side driver. Operating with sync FET body diode conducting.	B
HB	7	BIAS	Possible damage. HB exceeds absolute maximum voltage rating	A
BIAS	8	VCC	Possible damage to VCC if BIAS is above the absolute maximum voltage rating of VCC, otherwise no damage	A
VCC	9	PGND	No VCC rail, no switching	B
PGND	10	LO	LO never turns on. Switching never happens	B
LO	11	MODE	Switching mode toggles with every switching cycle	C
MODE	12	UVLO/EN	Switching mode set by the UVLO/EN pin voltage	B
UVLO/EN	13	SYNC/ DITHER/VH	SYNC/DITHER/VH setting set by the UVLO/EN pin	B
SYNC/ DITHER/VH	14	RT	Can exceed the RT absolute maximum voltage	A
RT	15	VREF/RANGE	Switching frequency will not be correct	C
VREF/RANGE	16	SS	Small soft-start time	C
SS	17	TRK	TRK > 1.2V will stop any switching on the controller.	B
TRK	18	AGND	VOUT out of regulation, no switching	B
AGND	19	COMP	VOUT out of regulation, not switching.	B
COMP	20	CSP	Possible damage. Exceeds absolute maximum voltage rating of COMP	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to 12 V supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CSP	1	Normal operation	D
CSN	2	Loss of current sense signal. Circuit possibly unstable	C
VOUT/SENSE	3	VOUT out of regulation	B
PGOOD	4	Loss of PGOOD functionality	C
HO	5	HO pin can exceed the HO to SW absolute maximum voltage rating	A
SW	6	No energy is transferred from input to output	B
HB	7	HB exceeds HB to SW absolute maximum voltage rating	A
BIAS	8	Normal operation	D
VCC	9	VCC exceeds absolute maximum voltage rating	A
PGND	10	Possible damage	A
LO	11	Possible damage. Exceeds absolute maximum voltage rating	A
MODE	12	Possible damage. Exceeds absolute maximum voltage rating	A
UVLO/EN	13	No UVLO functionality	C
SYNC/ DITHER/VH	14	Possible damage. Exceeds absolute maximum voltage rating	A
RT	15	Possible damage. Exceeds absolute maximum voltage rating	A
VREF/RANGE	16	Possible damage. Exceeds absolute maximum voltage rating	A
SS	17	Possible damage. Exceeds absolute maximum voltage rating	A
TRK	18	Possible damage. Exceeds absolute maximum voltage rating	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to 12 V supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
AGND	19	Possible damage. Exceeds absolute maximum voltage rating	A
COMP	20	Possible damage. Exceeds absolute maximum voltage rating	A

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