Functional Safety Information

TCAL9539-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

Copyright © 2023 Texas Instruments Incorporated

1 Overview

This document contains information for the TCAL9539-Q1 (WQFN RTW package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 andFigure 1-2 show the device functional block diagrams for reference.

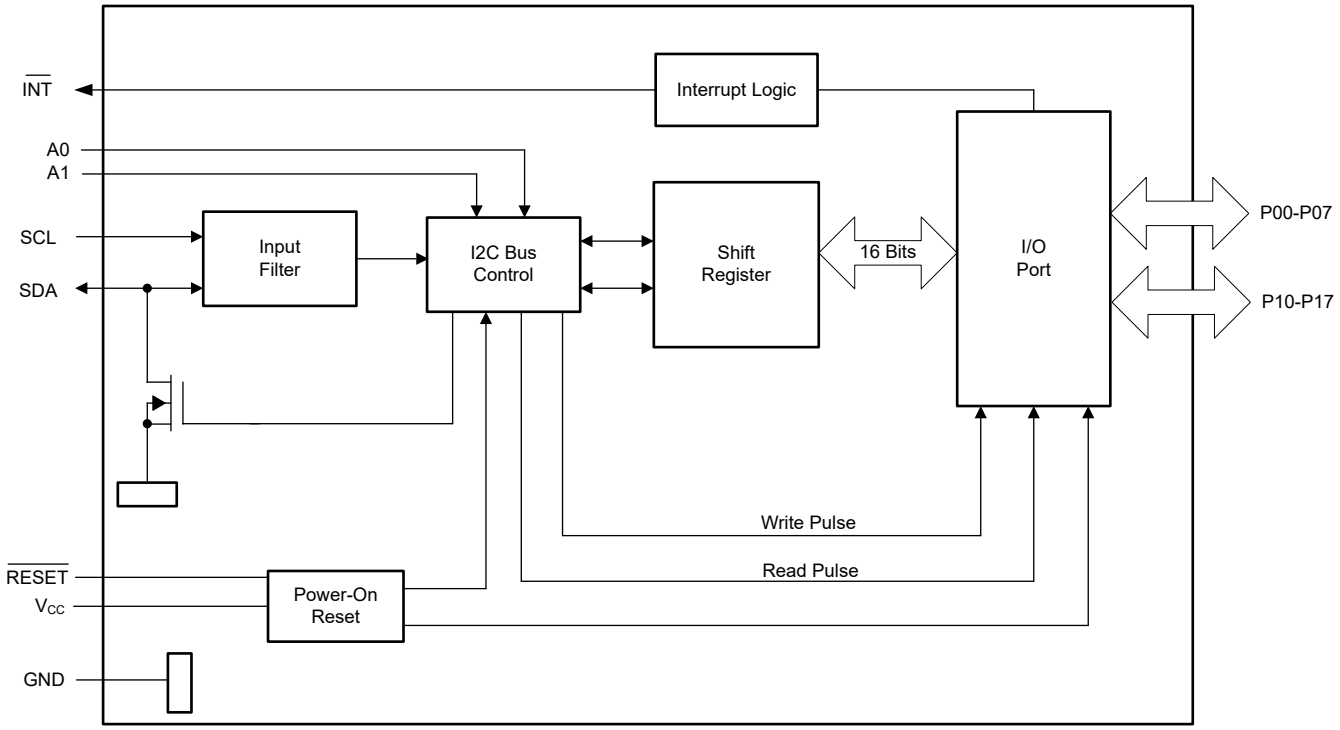

Figure 1-1. Functional Block Diagram

Copyright © 2023 Texas Instruments Incorporated

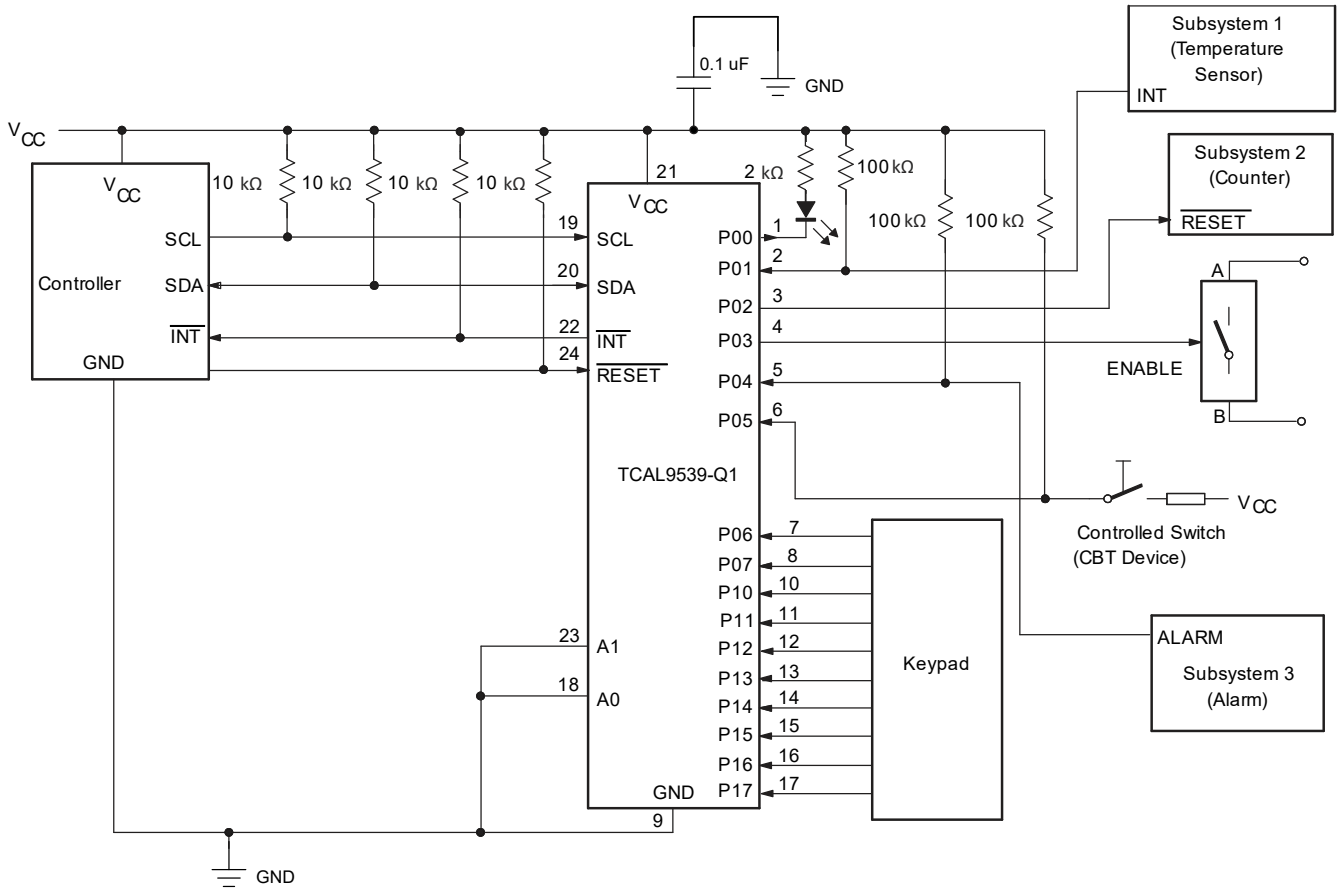

Figure 1-2. Simplified Schematic of P00 to P17

The TCAL9539-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

Copyright © 2023 Texas Instruments Incorporated

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TCAL9539-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	2
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 35 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

Copyright © 2023 Texas Instruments Incorporated

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TCAL9539-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
I2C control / communication error	40
I/O configuration error	30
I/O data bit error	25
INT false trip, fails to trip	5

Copyright © 2023 Texas Instruments Incorporated

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TCAL9539-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TCAL9539-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TCAL9539-Q1 data sheet.

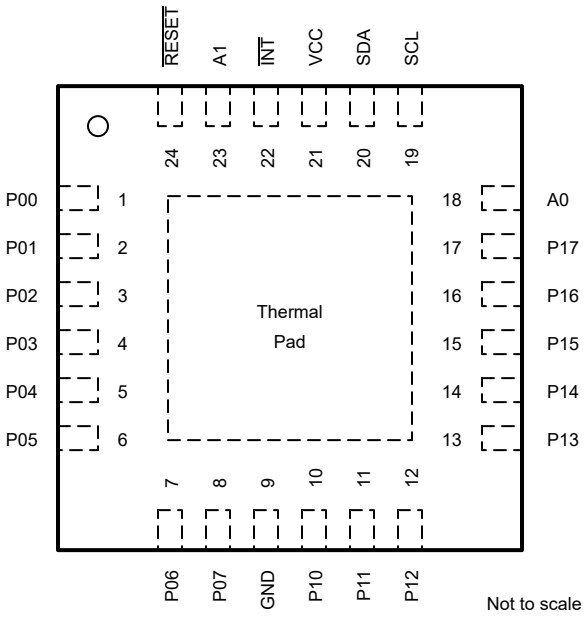

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption SDA/SCL/RESET/INT/PXX are pulled high with an external pull up resistor

Copyright © 2023 Texas Instruments Incorporated

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P00	1	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P01	2	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P02	3	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P03	4	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P04	5	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P05	6	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P06	7	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P07	8	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
GND	9	GND shorted to GND, no issues expected	D
P10	10	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P11	11	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P12	12	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P13	13	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P14	14	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P15	15	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P16	16	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
P17	17	Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected.	A
A0	18	Device address A0 forced low, potential functionality lost if state was previously high. No device harm expected	B
SCL	19	SCL stuck low resulting in functionality lost, no device damage expected. I2C bus would be stuck on the system level	B
SDA	20	SDA stuck low resulting in functionality lost, no device damage expected. I2C bus would be stuck on the system level	B
VCC	21	Device would be held in reset and all functionality would be lost. All PXX pins would become HIGH-Z.	B

Copyright © 2023 Texas Instruments Incorporated

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
#INT	22	INT stuck low resulting in functionality loss, no device damage/harm expected	B
A1	23	Device address A1 forced low, potential functionality lost if state was previously high. No device harm expected	B
#RESET	24	Device is held in RESET. No device harm expected, but functionality loss due to NACKs and p-ports remain HI-Z inputs.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P00	1	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P01	2	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P02	3	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P03	4	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P04	5	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P05	6	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P06	7	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P07	8	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
GND	9	Device is not biased to GND, potential damage to device may depending on if GND floats excessively high or low. Device functionality will be lost.	A
P10	10	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P11	11	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P12	12	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P13	13	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P14	14	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P15	15	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
P16	16	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B

Copyright © 2023 Texas Instruments Incorporated

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P17	17	If pin is configured to be an input, larger supply current may occur . May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost for both cases (GPIO set as an input or an output). No harm to device is expected.	B
A0	18	Device address could float and the device target address would be unknown (potential functional problem) and in worst case, it may become an address which is already occupied by another target device on the bus. No damage expected.	B
SCL	19	Larger supply current may occur due to this becoming a floating input. Functionality is lost due to I2C communication being cut off to this device. No damage expected. When trying to communicate to the device, I2C shows NACKs when address is trying to be called.	B
SDA	20	Larger supply current may occur due to this becoming a floating input. Functionality is lost due to I2C communication being cut off to this device. No damage expected. When trying to communicate to the device, I2C shows NACKs when address is trying to be called.	B
VCC	21	Functionality is lost.	B
#INT	22	The INT pin can no longer assert low, the processor is not informed of any INTs. No damage expected	B
A1	23	Device address could float and the device target address would be unknown (potential functional problem) and in worst case, it may become an address which is already occupied by another target device on the bus. No damage expected.	B
#RESET	24	Device pin may float to an unknown state, if floats to LOW then the device is held in reset and is unresponsive (functional issue). Potential spordaic behavior where device may respond and operate correctly or not work at all, may cause system level issues depending on what the GPIOs are tied to.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
P00	1	P01	If P00 and P01 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P00 and P01 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P00 and P01 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P00 and P01 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P01	2	P02	If P01 and P02 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P01 and P02 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P01 and P02 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P01 and P02 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A

Copyright © 2023 Texas Instruments Incorporated

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
P02	3	P03	If P02 and P03 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P02 and P03 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P02 and P03 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P02 and P03 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P03	4	P04	If P03 and P04 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P03 and P04 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P03 and P04 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P03 and P04 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P04	5	P05	If P04 and P05 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P04 and P05 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P04 and P05 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P04 and P05 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A

Copyright © 2023 Texas Instruments Incorporated

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
P06	7	P07	If P06 and P07 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P06 and P07 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P06 and P07 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P06 and P07 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P07	8	GND	If P07 is set to an OUTPUT LOW, no functionality or damage is expected. If P07 is an INPUT, no damage is expect, but functionality is lost as P07 will likely not see a logic HIGH and set the INT. If P07 is an OUTPUT HIGH, damage is likely to occur as a large IoH current flows from the pin and likely exceed the VoH limit.	A
GND	9	P10	If P10 is set to an OUTPUT LOW, no functionality or damage is expected. If P10 is an INPUT, no damage is expect, but functionality is lost as P10 will likely not see a logic HIGH and set the INT. If P10 is an OUTPUT HIGH, damage is likely to occur as a large IoH current flows from the pin and likely exceed the VoH limit.	A
P10	10	P11	If P10 and P11 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P10 and P11 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P10 and P11 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P10 and P11 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P11	11	P12	If P11 and P12 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P11 and P12 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P11 and P12 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P11 and P12 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A

Copyright © 2023 Texas Instruments Incorporated

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
P13	13	P14	If P13 and P14 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P13 and P14 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P13 and P14 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P13 and P14 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P14	14	P15	If P14 and P15 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P14 and P15 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P14 and P15 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P14 and P15 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P15	15	P16	If P15 and P16 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P15 and P16 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P15 and P16 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P15 and P16 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A

Copyright © 2023 Texas Instruments Incorporated

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
P16	16	P17	If P16 and P17 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If IoH exceeds 10mA then damage may occur but may not be instantaneous. Failures over time may occur. If P16 and P17 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur. If P16 and P17 are both INPUTs, no damage is expected if both have the same pull-up or pull-down configuration. If opposite pull-up and pull-down configuration exists, excess current through the input buffers could take place leading to indeterminant IO state and false interrupts. If P16 and P17 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P17	17	A0	If P17 is an INPUT, no expected damage. Functionality may be lost depending on what is connected to P17 in the system which is now also connected to A0. If P17 is an OUTPUT HIGH and A0 is referenced to a pull up to Vcc or if P17 is an OUTPUT LOW and A0 is referenced to a logic low, then no functionality or damage is expected. If P17 is an OUTPUT HIGH and A0 is referenced to a low through a resistor or P17 is an OUTPUT LOW and A0 is referenced to a logic HIGH through a resistor, then A0 will now be a different state than intended/designed for. The processor will not be able to access the intended I2C target. If another I2C target shares the same address as this device, then signal integrity issues may be a concern. Device may end up being programmed incorrectly/unintentionally in this case. Functionality may be lost due to this. Direct damage is not expected though depending on how the system implements the GPIOs, damage may be possible due to unintended programming.	A
SCL	19	SDA	I2C communication will be lost both to the device and to the system's I2C bus. Functionality is lost, but no damage expected.	B
SDA	20	VCC	Device is likely to be damaged during ACKs and read transaction due to large excessive current through pin. If IoL exceeds 6 mA at 85°C or less, device may be damaged. Damage may not be instanteous but may occur over time. VoL from device may also be too large for master to accept as a valid low during ACKs.	A
Vcc	21	#INT	If INT is de-asserted/HIGH then there should not be concerns outside of potential leakage currents. When INT asserts, large IoL current flows from VCC to GND through the INT pin, if VCC of device is low then the NFET (of INT) saturates and VoL on INT clamps as well as the IoL current. Damage may occur, but may not break the device instantly, likely damage over time. From a system level, processor looking at the INT may not see an interrupt as the VoL could be larger than the ViL of a processor.	A

Copyright © 2023 Texas Instruments Incorporated

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
#INT	22	A1	Device address may change if A1 is tied to a pull-up resistor whenever INT asserts. Address would change back when INT de-asserts. If A1 is tied to a pull-down resistor, voltage at A1 may be at a mid voltage due to resistor divider between A1's pull down and INT's pull-up. Address of device may change due to any noise/coupling onto the pin. Increased leakage current on supply would be seen. When INT asserts, the address will set back to low. INT may also never go above ViH for any processor/mcu looking at the INT line. Additional leakage current may be expected at the processor/mcu input for the INT. Functionality may be lost.	B
A1	23	#RESET	If A1 is tied to a pull-down resistor, A1 and RESET will form a voltage divider and the voltage at these pins will settle somewhere mid rail if pull-up and pull-down resistors are equal in value. RESET and device address may be in an unknown state because they are not above/below ViH/ViL levels. Noise coupling onto these pins may toggle reset. Assume functionality is lost. If A1 is tied HIGH and we assume RESET is tied HIGH with pull-up resistors, no errors are expected.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P00	1	If P00 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P00 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P00 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P01	2	If P01 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P01 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P01 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P02	3	If P02 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P02 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P02 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P03	4	If P03 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P03 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P03 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P04	5	If P04 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P04 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P04 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A

Copyright © 2023 Texas Instruments Incorporated

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P05	6	If P05 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P05 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P05 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P06	7	If P06 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P06 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P06 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P07	8	If P07 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P07 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P07 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
GND	9	Device may be damaged due to biasing of internal substrates which were previously only supposed to be biased to GND.	A
P10	10	If P10 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P10 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P10 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P11	11	If P11 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P11 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P11 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P12	12	If P12 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P12 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P12 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P13	13	If P13 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P13 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P13 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P14	14	If P14 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P14 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P14 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P15	15	If P15 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P15 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P15 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A

Copyright © 2023 Texas Instruments Incorporated

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P16	16	If P16 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P16 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P16 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
P17	17	If P17 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P17 is set to an OUTPUT LOW, then large current from VCC to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P17 is set to an INPUT, then there should be no concerns outside of leakage currents. Note functionality of the input will be lost because P00 will be held HIGH and will not ever go low.	A
A0	18	If A0 is tied to a pull up voltage, then there should be no concerns outside of leakage currents. If A0 is referenced to GND with a pull up resistor, then the device will now interpret A0 as a logic HIGH and the I2C Controller will not be able to communicate to the device (I2C target address has changed). If there is another device on the bus with the same address, then there could be signal integrity concerns or GPIOs could be set to the wrong settings. Worst case is A0 is tied directly to GND. If VCC were shorted to A1 in this case, we would have a direct short to GND. No damage is expected to our device but may cause damage to power supplying rail	A
SCL	19	SCL is an input, so no damage is expected to the device. The device may not see a valid VoL though as the I2C controller will likely have a larger VoL due to the excess current. Worst case for device is lose of I2C communication due to VoL I2C controller> ViL device. Damage to the processor may occur or any device which supports clock stretching.	B
SDA	20	Device may be damaged during ACKs and read transaction due to large excessive current through pin. Damage may not be instanteous but may occur over time. VoL from device may also be too large for I2C Controller to accept as a valid low during ACKs.	A
VCC	21	VCC is shorted to VCC, this is expected and no damage should occur.	D
#INT	22	If INT is de-asserted/HIGH then there should not be concerns outside of potential leakage currents. When INT asserts, large IoL current flows from VCC to GND through the INT pin, if VCC of device is low then the NFET (of INT) saturates and VoL on INT clamps as well as the IoL current. Damage may occur, but may not break the device instantly, likely damage over time. From a system level, processor looking at the INT may not see an interrupt as the VoL could be larger than the ViL of a processor.	A
A1	23	If A1 is tied to a pull up voltage, then there should be no concerns outside of leakage currents. If A1 is referenced to GND with a pull up resistor, then the device interprets A1 as a logic HIGH and the master/processor is not able to communicate to the device (I2C target address has changed). If there is another device on the bus with the same address, then there could be signal integrity concerns or GPIOs could be set to the wrong settings. Worst case is A1 is tied directly to GND. If VCC were shorted to A1 in this case, ther is a direct short to GND. No damage is expected to our device, but may cause damage to power supplying rail	B
#RESET	24	If RESET is tied to a pull up voltage, then there should be no concerns outside of leakage currents. If processor or any external circuit attempts to drive #RESET low, it may see a large current from Vcc to GND. The external driver may be damaged. Device will not be able to be reset through this hardware pin.	B

Copyright © 2023 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated