Functional Safety Information

ISO1212 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for ISO1212 (16-DBQ package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

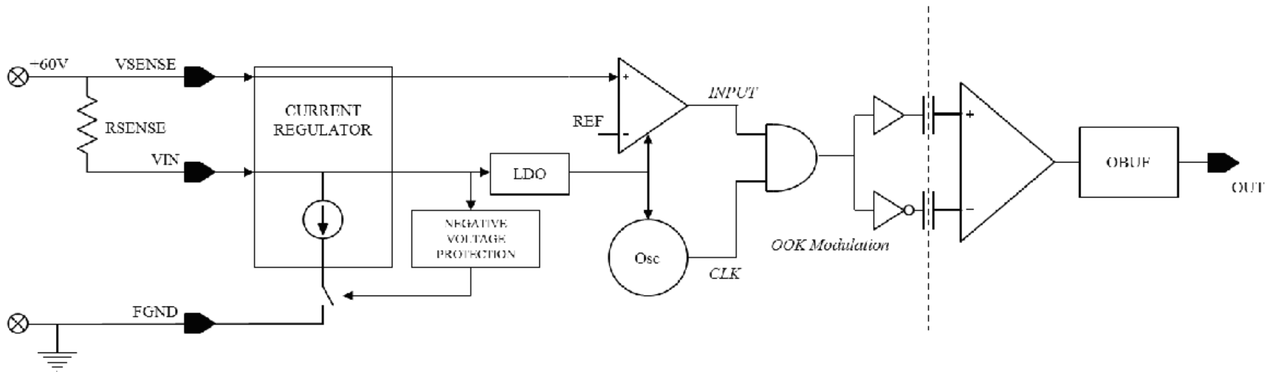

Figure 1-1. Functional Block Diagram

ISO1212 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 16-DBQ (SSOP) Package

This section provides functional safety failure in time (FIT) rates for 16-DBQ package of ISO1212 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	28
Die FIT rate	18
Package FIT rate	10

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 900mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	20 FIT	55 °C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO1212 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT state undetermined	38
OUT stuck to default state	34
OUT not in voltage or timing specification	17
OUT stuck high	4
OUT stuck low	4
OUT stuck to non-default state	3

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISO1212 (16-DBQ package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Note

When pin short to ground cases are discussed, only the same side ground shorts are considered.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

4.1 16-DBQ (SSOP) Package

Figure 4-1 shows the ISO1212 pin diagram for the 16-DBQ package. For a detailed description of the device pins please, see the *Pin Configuration and Functions* section in the ISO1212 data sheet.

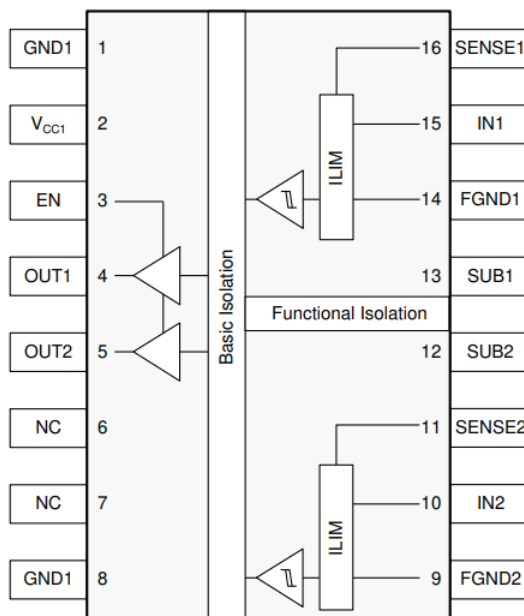

Figure 4-1. Pin Diagram (16-DBQ Package)

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND1	1	Device continues to function as expected.	D
V_{CC1}	2	No power to the device on the logic side. Verify that the *absolute maximum ratings* for all pins of the device are met; otherwise, device damage is plausible. OUT state undetermined.	A
EN	3	Disables the output buffer for OUT1 and OUT2. OUT1 and OUT2 are in a high impedance state.	B
OUT1	4	OUT1 is stuck low. Device damage is plausible if IN1 and SENSE1 causes OUT1 to stay high for an extended period of time.	A
OUT2	5	OUT2 is stuck low. Device damage is plausible if IN2 and SENSE2 causes OUT2 to stay high for an extended period of time.	A
NC	6	Device continues to function as expected.	D
	7	Device continues to function as expected.	D
GND1	8	Device continues to function as expected.	D
FGND2	9	FGND2 is shorted to FGND2. Device continues to function as expected.	D
IN2	10	IN2 is shorted to FGND2 and device damage is plausible.	A
SENSE2	11	SENSE2 is shorted to FGND2 and device damage is plausible.	A
SUB2	12	Substrate2 is shorted to FGND2. A negative potential in IN2 and SENSE2 pins can cause permanent damage.	A
SUB1	13	Substrate1 shorted to FGND1. A negative potential in IN1 and SENSE1 pins can cause permanent damage.	A
FGND1	14	FGDN1 is shorted to FGND1. Device continues to function as expected.	D
IN1	15	IN1 is shorted to FGND1 and device damage is plausible.	A
SENSE1	16	SENSE1 is shorted to FGND1 and device damage plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND1	1	Device receives return ground through pin8. Normal operation.	D
V_{CC1}	2	Device is not powered up. If EN is high, then current can flow through ESD to VCC1 and cause damage.	A
EN	3	Control on OUT1 and OUT2 output is lost but the field side data from IN and SENSE to OUT channels continues normally.	B
OUT1	4	State of OUT1 is undetermined. Field side data from IN and SENSE to OUT is lost.	B
OUT2	5	State of OUT2 is undetermined. Field side data from IN and SENSE to OUT is lost.	B
NC	6	Device continues to function as expected.	D
	7	Device continues to function as expected.	D
GND1	8	Device receives return ground through pin1. Normal operation.	D
FGND2	9	No return ground for field side-2.	B
IN2	10	No device damage but there is loss of critical functionality.	B
SENSE2	11	No device damage but there is loss of critical functionality.	B
SUB2	12	Substrate2 is open as expected. Normal operation.	D
SUB1	13	Substrate1 is open as expected. Normal operation.	D
FGND1	14	No return ground for field side-1.	B
IN1	15	No device damage but there is loss of critical functionality.	B
SENSE1	16	No device damage but there is loss of critical functionality.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effects	Failure Effect Class
GND1	1	V_{CC1}	No power to the device on the logic side. Verify that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is plausible.	A
V_{CC1}	2	EN	Externally, the V_{CC1} supply and EN driver output is shorted when V_{CC1} and EN is supplied and the logic high level and OUT is enabled and functions as expected. This function is dependent on the V_{CC1} and EN pin level results of the device. If V_{CC1} and EN is not supplied and low then OUT is not enabled and the output is off.	B
EN	3	OUT1	Device damage is plausible.	A
OUT1	4	OUT2	OUT1 and OUT2 might not reflect to IN1 and SENSE1 and IN2 and SENSE2, respectively. With the opposite logic state on both outputs, high current can flow between supply and ground and cause device damage.	A
OUT2	5	NC	Device continues to function as expected.	D
NC	6	NC	Device continues to function as expected.	D
NC	7	GND1	Device continues to function as expected.	D
GND1	8	NC	Device continues to function as expected.	D
FGND2	9	IN2	FGND2 shorted to IN2 and device damage is plausible.	A
IN2	10	SENSE2	IN2 shorted to SENSE2 and device damage is plausible.	A
SENSE2	11	SUB2	No device damage but there is loss of critical functionality.	B
SUB2	12	SUB1	No device damage but there is loss of critical functionality.	B
SUB1	13	FGND1	Substrate1 shorted to FGND1 and device damage is plausible.	A
FGND1	14	IN1	FGND1 shorted to IN1 and device damage is plausible.	A
IN1	15	SENSE1	IN1 shorted to SENSE1 and device damage is plausible.	A
SENSE1	16	IN1	IN1 shorted to SENSE1 and device damage is plausible.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND1	1	Causes high current to flow in the device and device damage is plausible.	A
V_{CC1}	2	No effect. Normal operation.	D
EN	3	Control to disable OUT1 and OUT2 is lost. OUT1 and OUT2 behaves as expected.	B
OUT1	4	OUT1 is stuck high. Data communication from IN1 and SENSE1 to OUT1 is lost. Device damage is plausible if IN1 and SENSE1 causes OUT1 to be low.	A
OUT2	5	OUT2 is stuck high. Data communication from IN2 and SENSE2 to OUT2 is lost. Device damage is plausible if IN2 and SENSE2 causes OUT2 to be low.	A
NC	6	Device continues to function as expected.	D
	7	Device continues to function as expected.	D
GND1	8	Causes high current to flow in the device and device damage is plausible.	A
FGND2	9	FGND2 shorted to V_{CC1}. Causes high current to flow in the device and device damage is plausible.	A
IN2	10	IN2 is shorted to V_{CC1} and device damage is plausible.	A
SENSE2	11	SENSE2 is shorted to V_{CC1} and device damage is plausible.	A
SUB2	12	Substrate2 is shorted to V_{CC1} and device damage is plausible.	A
SUB1	13	Substrate1 is shorted to V_{CC1} and device damage is plausible.	A
FGND1	14	FGND1 is shorted to V_{CC1}. Causes high current to flow in the device and device damage is plausible.	A
IN1	15	IN1 is shorted to V_{CC1} and device damage is plausible.	A
SENSE1	16	SENSE1 is shorted to V_{CC1} and device damage is plausible.	A

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