Functional Safety Information

LM5164
Functional Safety FIT Rate, FMD, and Pin FMA

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Trademarks

1 Overview

This document contains information for LM5164 (SO PowerPad™ integrated circuit package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

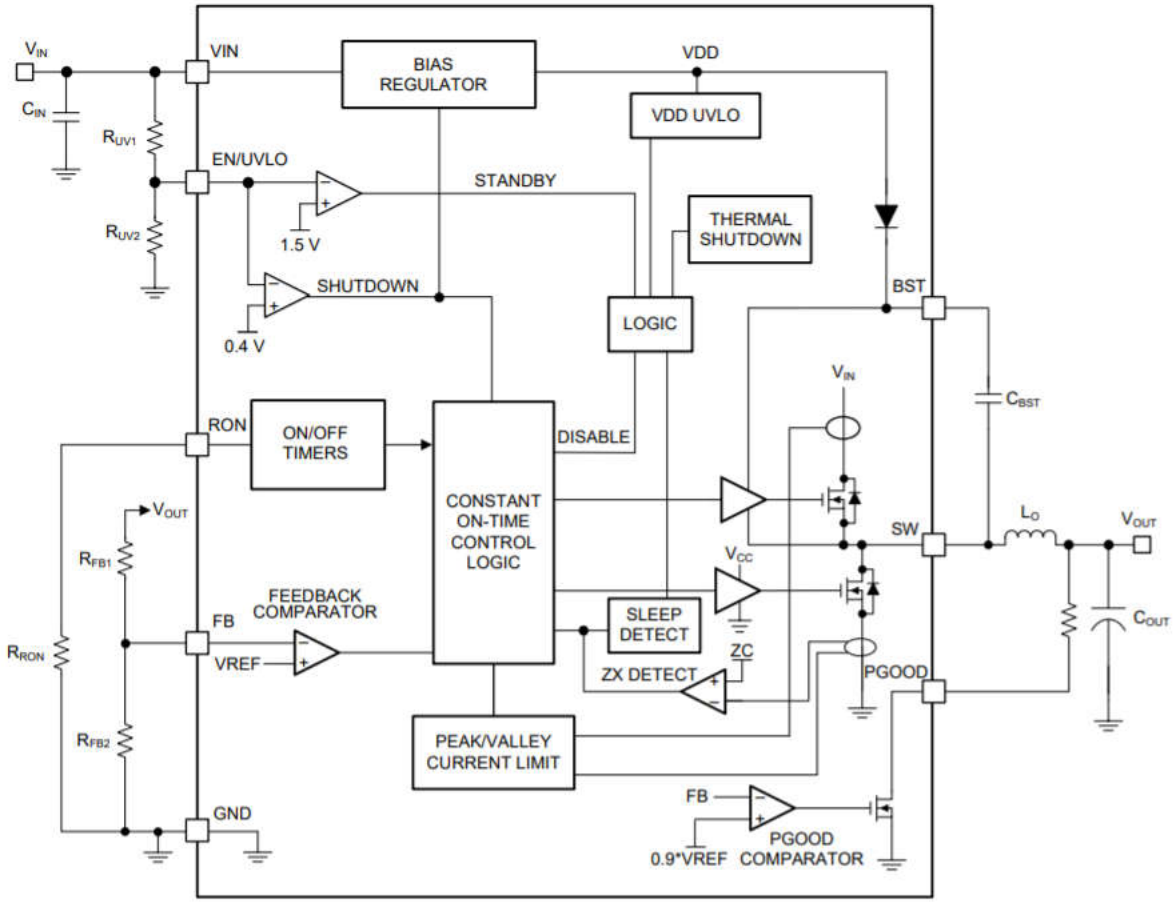

Figure 1-1. Functional Block Diagram

LM5164 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM5164 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	5
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 700mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV > 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5164 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No SW output	45
SW output not in specification – voltage or timing	40
SW power FET stuck on	5
PGOOD false trip, fails to trip	5
Short circuit any two pins	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5164. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM5164 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM5164 datasheet.

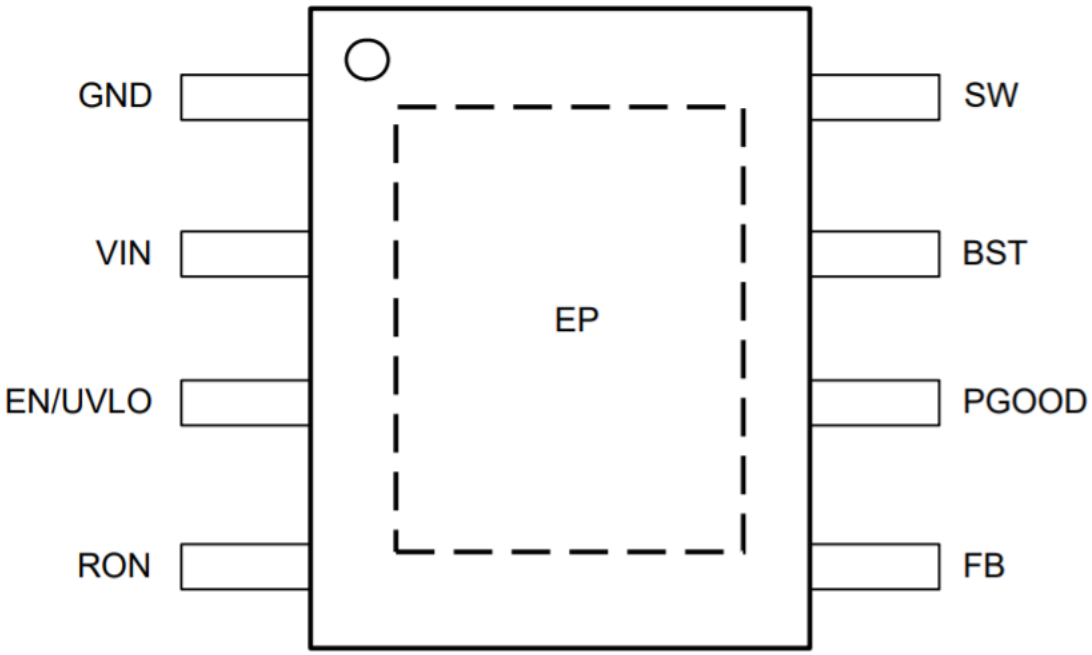

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The application circuit is configured per the LM5164 datasheet.
  - The PGOOD pin is pulled up to VOUT.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	N/A	D
VIN	2	VOUT = 0V.	B
EN/UVLO	3	VOUT = 0V.	B
RON	4	VOUT is unregulated; 0 ≤ VOUT < set voltage.	B
FB	5	VOUT > set voltage. The PGOOD pin can become damaged if VIN > 14V.	A
PGOOD	6	The flag of the PGOOD pin is invalid.	B
BST	7	VOUT = 0V.	B
SW	8	The power FET is damaged.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	VOUT = 0V.	B
VIN	2	VOUT = 0V.	B
EN/UVLO	3	VOUT = 0V.	B
RON	4	VOUT > set voltage.	B
FB	5	VOUT > set voltage. The PGOOD pin can become damaged if VIN > 14V.	A
PGOOD	6	The flag of the PGOOD pin is invalid.	B
BST	7	VOUT = 0V.	B
SW	8	VOUT = 0V.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Short to	Description of Potential Failure Effects	Failure Effect Class
GND	1	VIN	The input is grounded. The device is disabled. VOUT = 0V.	B
VIN	2	EN/UVLO	There is no impact on functionality.	D
EN/UVLO	3	RON	The device is potentially disabled.	B
			The device potentially operates at an incorrect frequency if the EN pin is connected to the VIN pin through a resistor, depending on the resulting voltage of the EN pin from the specific resistor network.	C
			The device is potentially damaged if the EN pin is directly shorted to the VIN pin.	A
RON	4	N/A	N/A	D
FB	5	PGOOD	There is no impact on functionality if there is no external pullup at the PGOOD pin.	D
			VOUT is potentially lower than the set-point if an external pullup exists at the PGOOD pin.	C
PGOOD	6	BST	The device cannot start up due to the pulldown of the PGOOD pin, which prevents the BST voltage from being established. VOUT = 0V.	B
			When the short occurs during operation, the PGOOD pin is potentially damaged if the absolute maximum voltage rating of the PGOOD pin is exceeded.	A
BST	7	SW	Boot voltage cannot be established, and the device is disabled. VOUT = 0V.	B
			VOUT potentially equals the internal VDD (5V) minus the diode drop of the internal boot diode if the output rail is an open circuit.	B
			VOUT potentially drops to 0V if the load exceeds the internal VDD of the current limit of the LDO. VOUT = 0V.	B
SW	8	N/A	N/A	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
GND	1	VOUT = 0V.	B
VIN	2	N/A	D
EN/UVLO	3	N/A	D
RON	4	VIN > 5.5V can lead to device damage.	A
FB	5	VIN > 5.5V can lead to device damage.	A
PGOOD	6	VIN > 14V can lead to device damage.	A
BST	7	VOUT = 0 V.	B
SW	8	VOUT = VIN. The PGOOD pin can be damaged if VIN > 14V.	A

5 Revision History

Changes from February 3, 2022 to December 16, 2025 (from Revision * (February 2022) to Revision A (December 2025)) **Page**

- Added PowerPad trademark throughout the document..... 2
- Updated the *Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11* table..... 3
- Updated tables in the *Pin Failure Mode Analysis (Pin FMA)* tables..... 5

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