Functional Safety Information

TPSM5601R5 and TPSM5601R5S Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPSM5601R5 and TPSM5601R5S (B3QFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

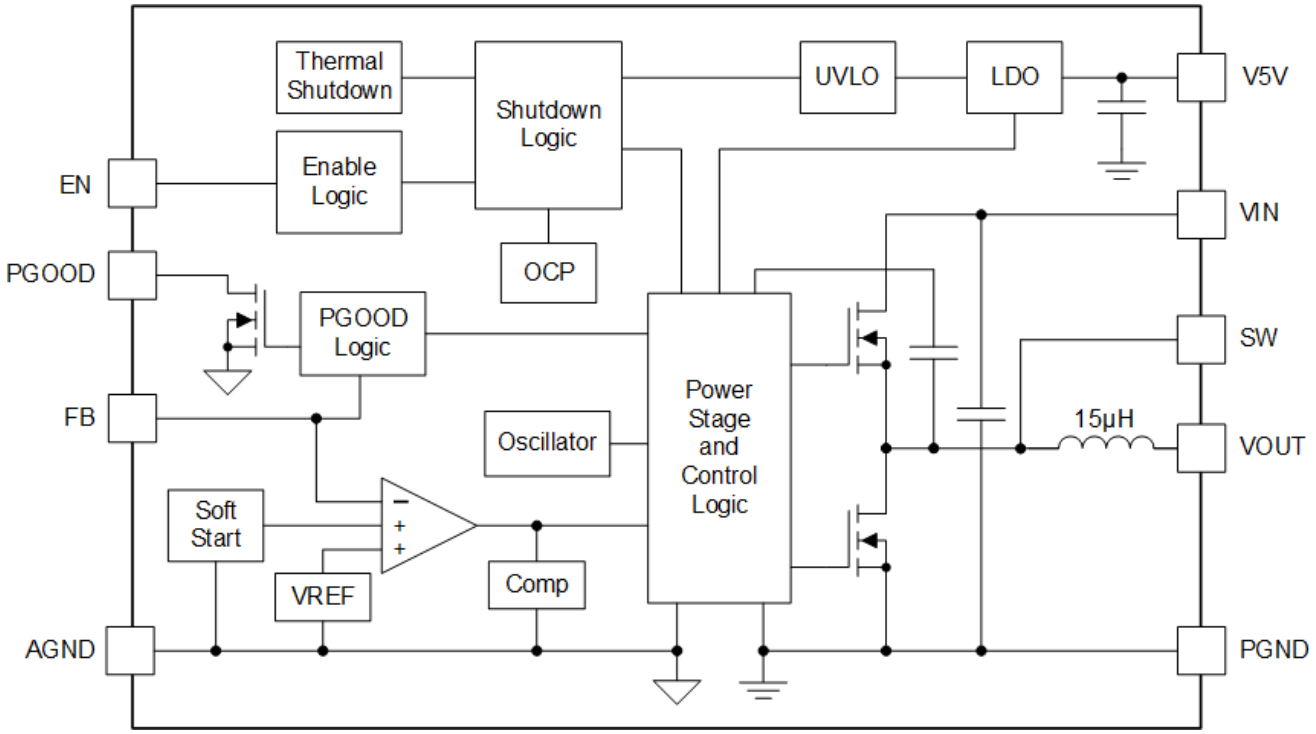

Figure 1-1. Functional Block Diagram

TPSM5601R5 and TPSM5601R5S were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPSM5601R5 and TPSM5601R5S based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	22
Die FIT Rate	4
Package FIT Rate	9
Passives FIT Rate	9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPSM5601R5 and TPSM5601R5S in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	60%
Output not in specification - voltage or timing	25%
Gate driver stuck on	5%
Power Good - False trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPSM5601R5 and TPSM5601R5S. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPSM5601R5 and TPSM5601R5S pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPSM5601R5 and TPSM5601R5S data sheet.

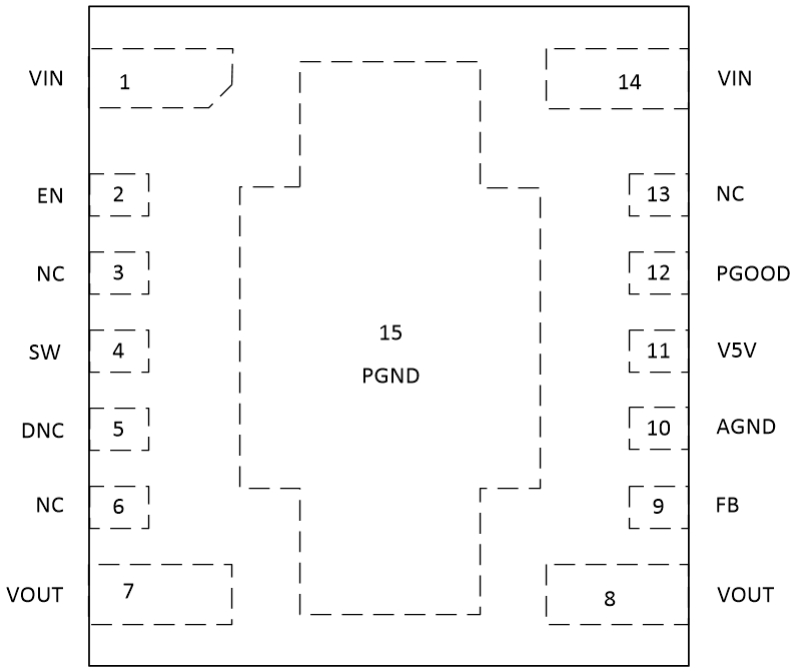

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the TPSM5601R5 and TPSM5601R5S data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 14	No output voltage will be generated. Possible damage to customer input supply, PCB can occur unless customer provides protection, or both. Reverse current from the SW pin to VIN pin, due to discharge of output capacitors, can damage regulator.	B
EN	2	This is a valid connection for the EN input. Enable functionality will be lost; the device will remain off with no output voltage generated. Damage to customer components connected to EN input can occur.	B
NC	3, 6, 13	Not connected to any circuitry within the module; no effect	D
SW	4	Shorting the SW pin to ground will result in large currents through the device and subsequent damage. No output voltage will be produced.	A
DNC	5	Driver supply to high side MOSFET will be lost. Output voltage will not be regulated. Possible damage to internal regulator and Cboot charging circuit	A
VOUT	7, 8	Loss of output voltage	B
FB	9	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage level. Possible damage to customer load, output stage components can occur, or both.	B
AGND	10	This is the ground pin, no effect	D
V5V	11	Internal circuits will be disabled. No output voltage will be generated. Possible increase in input current and possible damage to internal LDO	A
PGOOD	12	This is a valid connection for the PG output. PG functionality will be lost. Damage to customer components connected to PG input can occur.	D
PGND	15	This is the ground pin, no effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 14	Loss of output voltage	B
EN	2	Loss of enable functionality. Erratic operation; probable loss of regulation	B
NC	3, 6, 13	Not connected to any circuitry within the module; no effect	D
SW	4	This is a valid connection for the SW node; no effect	D
DNC	5	This is a valid connection for DNC pin; no effect	D
VOUT	7, 8	Loss of output voltage	B
FB	9	Device will not regulate. Output voltage can rise or fall. Damage to customer load, output stage components is probable, or both.	B
AGND	10	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load	B
V5V	11	This is a valid connection for V5V pin; no effect	D
PGOOD	12	This is a valid connection for the PGOOD output. PGOOD functionality will be lost.	B
PGND	15	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	EN	This is a valid connection for VIN. Enable functionality will be lost, the device will remain on.	D
EN	2	NC	Loss of enable functionality. Erratic operation; probable loss of regulation	B
NC	3	SW	NC pin not connected to any circuitry within the module; no effect	D
SW	4	DNC	Large currents will flow through internal circuits. Possible damage to internal regulator and CBOOT charging circuits. No output voltage will be produced.	A
DNC	5	NC	NC pin is not connected to any circuitry within the module; no effect	D
NC	6	VOUT	NC pin is not connected to any circuitry within the module; no effect	D
VOUT	7	PGND	Loss of output voltage	B
VOUT	8	FB	Erratic operation; loss of regulation. Possible damage to internal circuits will occur for VOUT > 5.5 V.	A
FB	9	AGND	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage level. Possible damage to customer load, output stage components can occur, or both.	B
AGND	10	V5V	Internal circuits will be disabled. No output voltage will be generated. Possible increase in input current and possible damage to internal LDO	A
V5V	11	PGOOD	Possible damage to internal circuitry	A
PGOOD	12	NC	No effect	D
NC	13	VIN	Normal operation; no effect	D
VIN	14	PGND	No output voltage will be generated. Possible damage to customer input supply, PCB can occur unless customer provides protection, or both. Reverse current from the SW pin to VIN pin, due to discharge of output capacitors, can damage the regulator.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 14	Normal operation	D
EN	2	Normal operation; enable functionality will be lost, the device will remain on.	D
NC	3, 6, 13	Normal operation	D
SW	4	Damage to the LS FET	A
DNC	5	VOUT = 0 V. CBOOT ESD clamp will run current to destruction.	A
VOUT	7, 8	Damage to LS FET. The output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A
FB	9	If VIN exceeds 5.5 V, damage will occur. VOUT = 0 V	A
AGND	10	VOUT = 0 V. Damage to other pins referred to GND	A
V5V	11	If VIN exceeds 5.5 V, damage will occur.	A
PGOOD	12	Damage to internal circuits	A
PGND	15	VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND	A

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