Functional Safety Information

UCC25800-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for UCC25800-Q1 (DGN-8 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

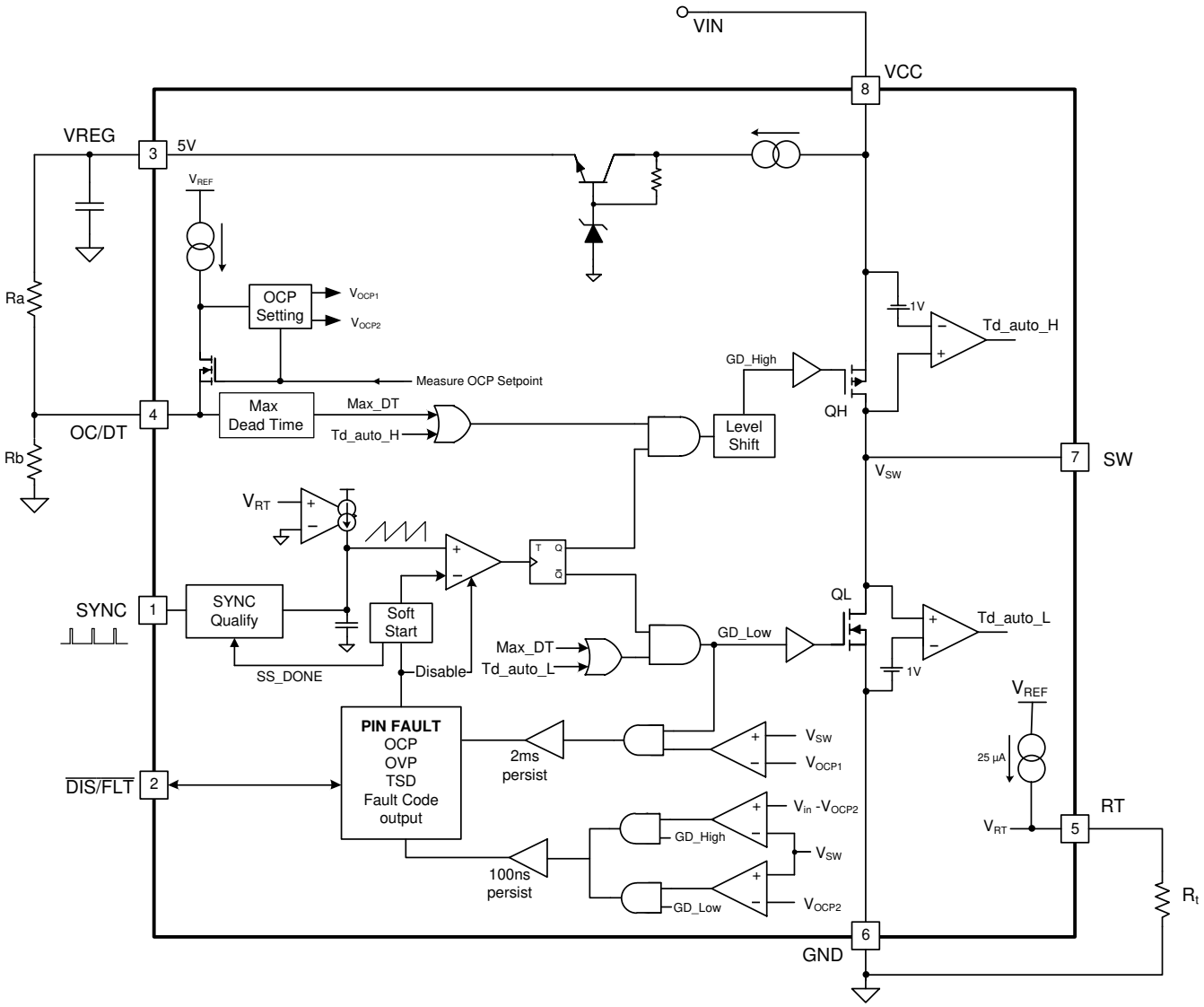

Figure 1-1. Functional Block Diagram

UCC25800-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC25800-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (125 mW, 250 mW, 500mW)	7, 8, 9
Die FIT Rate (125 mW, 250 mW, 500mW)	3, 4, 5
Package FIT Rate (125 mW, 250 mW, 500mW)	4, 4, 4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 125 mW, 250 mW, 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC25800-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW pin not switching	34
SW pin frequency out of specification	25
SW pin duty cycle out of specification	17
No effect	24

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC25800-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC25800-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC25800-Q1 data sheet.

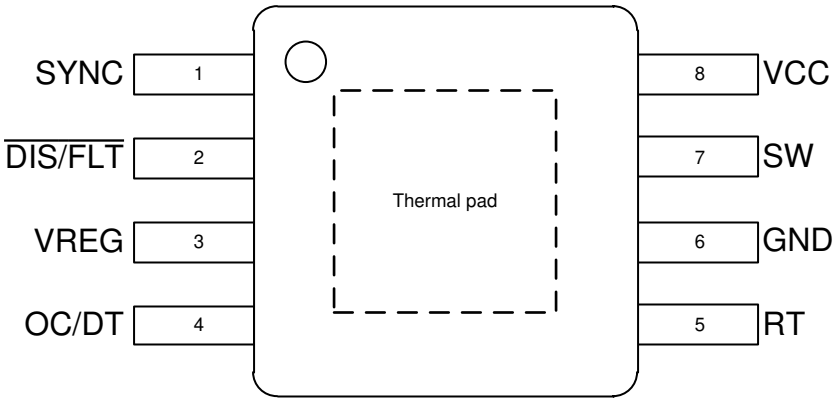

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section: The UCC25800-Q1 is connected based on UCC25800-Q1 EVM schematic, shown in Figure 3-1 of the User's Guide.

- SYNC pin is connected with 51-Ω to GND
- No external signal source applied to SYNC pin
- $\overline{\text{DIS/FLT}}$ pin is floating
- Thermal Pad is shorted to GND

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SYNC	1	Normal operation with programmed frequency.	D
$\overline{\text{DIS/FLT}}$	2	Device is disabled. No operation.	B
VREG	3	Device is disabled. No operation.	B
OC/DT	4	Device is disabled. No operation.	B
RT	5	Device is disabled. No operation.	B
GND	6	No effect.	D
SW	7	OCP2 triggered. Possible device damage.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	8	Device is not biased. No operation.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SYNC	1	No effect.	D
$\overline{\text{DIS/FLT}}$	2	No effect.	D
VREG	3	VREG open protection. No operation.	B
OC/DT	4	OC/DT open protection. No operation.	B
RT	5	Converter operates with 1.2-MHz switching frequency.	C
GND	6	No operation. Possible device damage	D
SW	7	Device operates normally. But converter has no output.	B
VCC	8	Device is not biased. No operation.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SYNC	1	$\overline{\text{DIS/FLT}}$	Device is disabled. No operation.	B
$\overline{\text{DIS/FLT}}$	2	VREG	No effect.	D
VREG	3	OC/DT	Device is disabled. No operation.	B
OC/DT	4	N/A	N/A	N/A
RT	5	GND	Device is disabled. No operation.	B
GND	6	SW	OCP2 triggered. Possible device damage.	A
SW	7	VCC	OCP2 triggered. Possible device damage.	A
VCC	8	N/A	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SYNC	1	Possible device damage.	A
$\overline{\text{DIS/FLT}}$	2	Possible device damage.	A
VREG	3	Possible device damage.	A
OC/DT	4	Possible device damage.	A
RT	5	Possible device damage.	A
GND	6	Device is not biased. No operation.	B
SW	7	OCP2 triggered. Possible device damage.	A
VCC	8	No effect.	D

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