Functional Safety Information

UCC27200-Q1, UCC2720xA-Q1, and UCC2721xA-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

PowerPAD™ is a trademark of Texas Instruments.
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1 Overview

This document contains information for the following device and package combinations to aid in a functional safety system design:

- UCC27200-Q1, UCC27202A-Q1, UCC27211A-Q1, and UCC27212A-Q1 (SOIC PowerPAD™ integrated circuit package)
- UCC27211A-Q1 (SOIC package)

Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

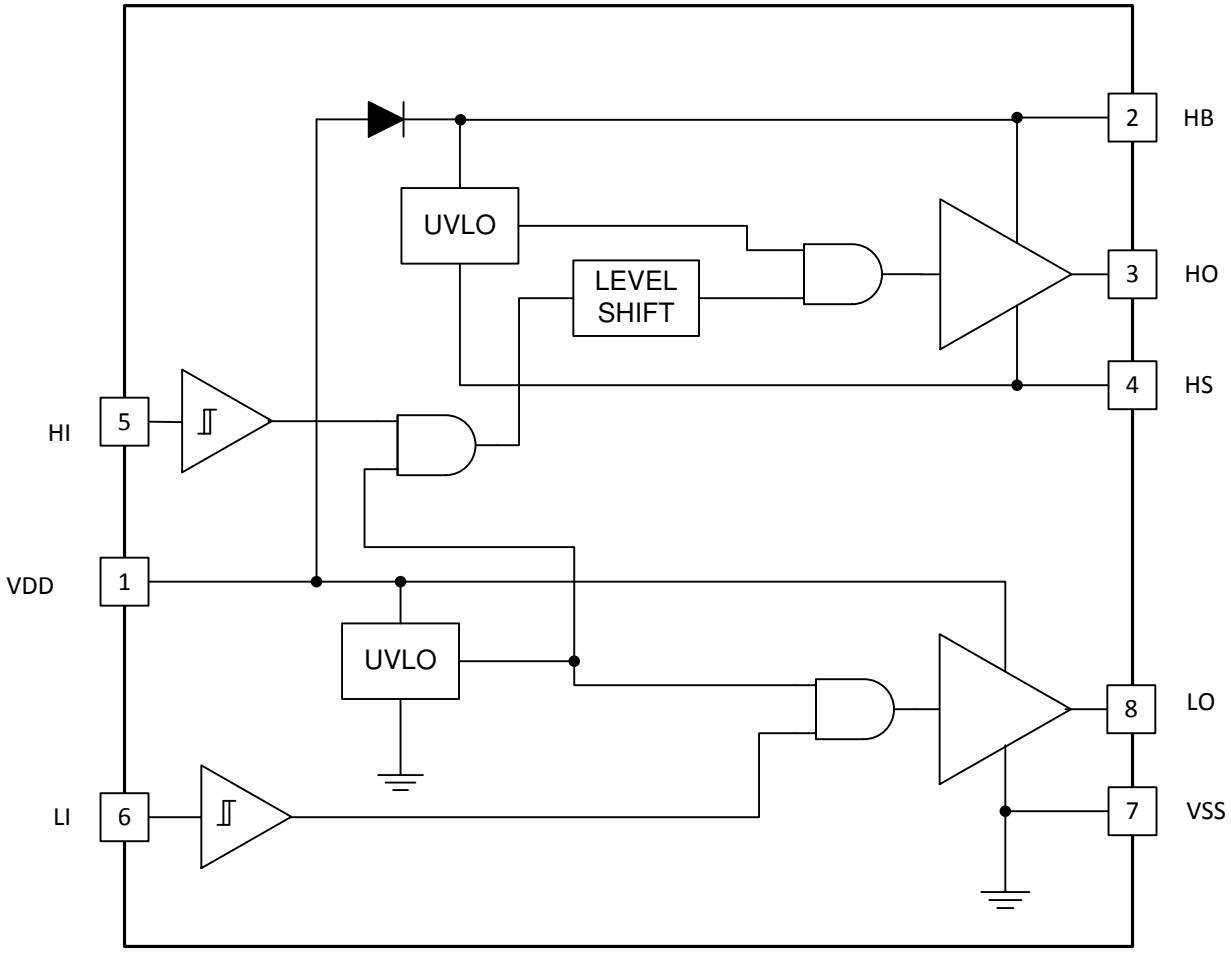

Figure 1-1. Functional Block Diagram

UCC27200-Q1, UCC2720xA-Q1, and UCC2721xA-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC PowerPAD™ Package

This section provides functional safety failure in time (FIT) rates for UCC27200-Q1, UCC27202A-Q1, UCC27211A-Q1, and UCC27212A-Q1 (SOIC PowerPAD™) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	50	10
	550	13
Die FIT rate	50	3
	550	5
Package FIT rate	50	7
	550	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 50mW, 550mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20	55

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOIC Package

This section provides functional safety failure in time (FIT) rates for UCC27211A-Q1 (SOIC) based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 1
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	50	10
	200	13
Die FIT rate	50	3
	200	5
Package FIT rate	50	7
	200	8

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 50mW, 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20	55

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC27200-Q1, UCC27202A-Q1, UCC27211A-Q1, and UCC27212A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO stuck low	16.3
HO stuck high	16.3
HO unknown or level is outside of specified level	16.3
LO stuck low	16.3
LO stuck high	16.3
LO unknown or level is outside of specified level	16.3
High side UVLO not functioning	1
Low side UVLO not functioning	1

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC27200-Q1, UCC27202A-Q1, UCC27211A-Q1, and UCC27212A-Q1 devices. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 and Figure 4-2 show the UCC27200-Q1, UCC27202A-Q1, UCC27211A-Q1, and UCC27212A-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC27200-Q1, UCC2720xA-Q1, and UCC2721xA-Q1 data sheets.

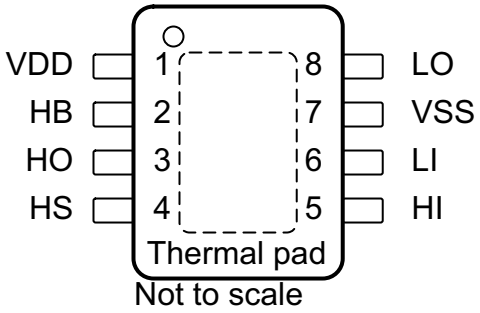

Figure 4-1. SOIC PowerPAD™ Pin Diagram

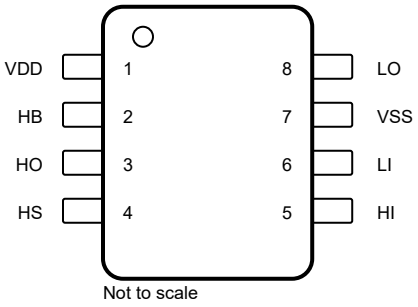

Figure 4-2. SOIC Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin 1 short to pin 8 is not considered.
- Pin 4 short to pin 5 is not considered.
- The case of short-circuited to supply is analyzed for short to VDD.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	Device power up is not possible. Device positive supply short to ground.	B
HB	2	Possible bootstrap diode damage. HO output is stuck low.	A
HO	3	Possible damage to HO output driver. HO output is stuck low.	A
HS	4	HO level is stuck low or ground level. High-side power FET can not pull up HO node.	B
HI	5	HO is stuck low.	B
LI	6	LO is stuck low.	B
VSS	7	No effect. Short to same potential.	D
LO	8	LO is stuck low. Possible LO output driver damage.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	Device power up is not possible. Device positive supply is open.	B
HB	2	High-side UVLO is detected. HO is stuck low.	B
HO	3	Power FET gate is disconnected from HO.	D
HS	4	HO output level is unknown.	B
HI	5	HO is stuck low.	B
LI	6	LO is stuck low.	B
VSS	7	No ground connection to the device. LO and HO are potentially pulled up to VDD level.	B
LO	8	Power FET gate is disconnected from HO.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDD	1	HB	High-side UVLO is detected. HO is stuck low.	B
HB	2	HO	Possible damage to bootstrap diode and HO output stage.	A
HO	3	HS	Possible damage to bootstrap diode and HO output stage.	A
HI	5	LI	HO and LO states depend on the driving source of LI and HI.	B
LI	6	VSS	LO is stuck low.	B
VSS	7	LO	LO is stuck low. Possible damage to LO output driver.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No effect. Short to same potential.	D
HB	2	High-side UVLO detection is possible. HO output level is lower than specified range and possibly stuck low if UVLO is detected.	B
HO	3	HO is stuck high at VDD level. Possible damage to HO driver.	A
HS	4	HO is stuck high at VDD level. Possible damage to HO driver.	A
HI	5	HO is stuck high.	B
LI	6	LO is stuck high.	B
VSS	7	Device power up is not possible. Device positive supply is short to ground.	B
LO	8	LO is stuck high at VDD level. Possible damage to LO driver.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 4, 2024 to September 18, 2025 (from Revision A (October 2024) to Revision B (September 2025)) **Page**

- Added the UCC27200-Q1 and UCC27202A-Q1 GPNs....2
- Updated trademark information....2
- Added clarifying language to the reliability data handbook reference....3

Changes from March 1, 2022 to October 3, 2024 (from Revision * (March 2022) to Revision A (October 2024)) **Page**

- Added package information for the non PowerPAD version of the SOIC package....2
- Updated FIT numbers....3
- Added package information for the non PowerPAD version of the SOIC package....4
- Added package image for the non PowerPAD version of the SOIC package diagram. 6

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