Functional Safety Information

UCC27517A-Q1 UCC27518A-Q1 UCC27519A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for UCC27517A-Q1 UCC27518A-Q1 UCC27519A-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

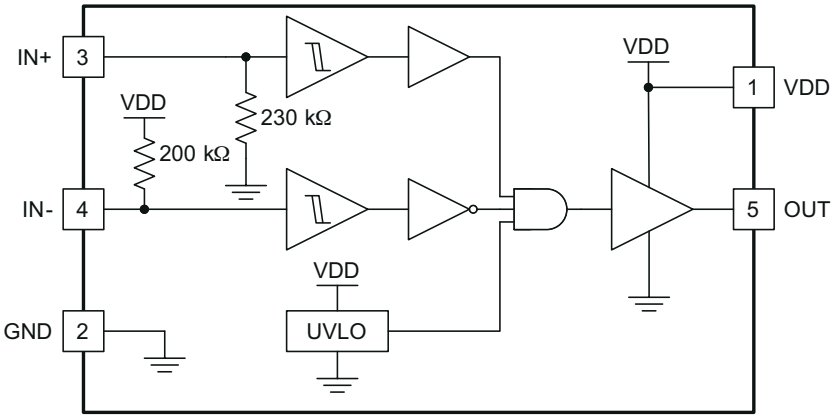

Figure 1-1. UCC27517A-Q1 Functional Block Diagram

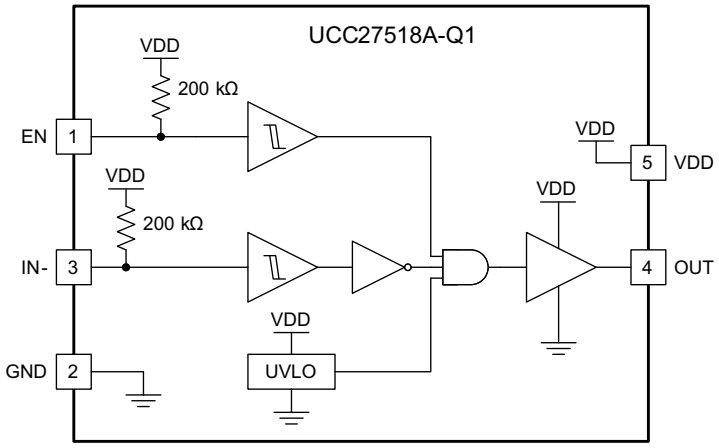

Figure 1-2. UCC27518A-Q1 Functional Block Diagram

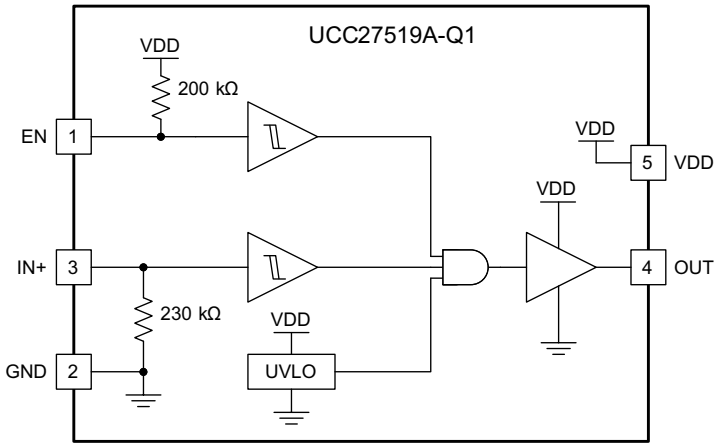

Figure 1-3. UCC27519A-Q1 Functional Block Diagram

UCC27517A-Q1, UCC27517A-Q1, and UCC27517A-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC27517A-Q1 UCC27518A-Q1 UCC27519A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (2,20,200mW)	2,2,3
Die FIT Rate(2,20,200mW)	5,5,12
Package FIT Rate(2,20,200mW)	3,3,9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 2,20,200mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC27517A-Q1 UCC27518A-Q1 UCC27519A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT Stuck high	33%
OUT Stuck low	33%
OUT not in spefified range	33%
UVLO not functioning	1%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC27517A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-4)
- Pin short-circuited to an adjacent pin (see Table 4-6)
- Pin short-circuited to supply (see Table 4-8)

Table 4-2 through Table 4-8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC27517A-Q1 UCC27518A-Q1 UCC27519A-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the data sheet.

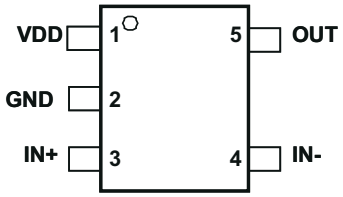

Figure 4-1. UCC27517A-Q1 Pin Diagram

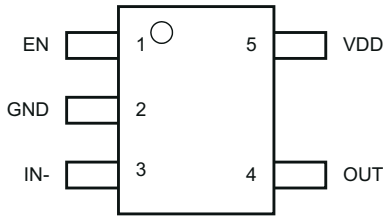

Figure 4-2. UCC27518A-Q1 Pin Diagram

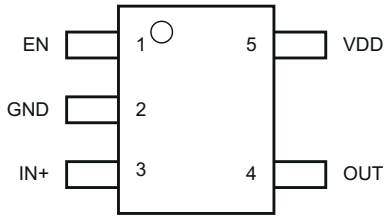

Figure 4-3. UCC27519A-Q1

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin #4 and 5 short case not considered.
- Short between corner pins are not considered.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	UCC27517A-Q1 Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	VDD and GND short circuit. No power is applied to the device.	D
GND	2	Short to same potential. No impact.	D
IN+	3	OUT stuck low.	B
IN-	4	OUT responds to IN+. IN- stuck low.	B
OUT	5	Posiible OUT pin and driver damge.	A

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	UCC27518A-Q1 UCC27519A-Q1Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	OUT is disabled	B
GND	2	Short to same potential. No impact.	D
IN-	3	OUT stuck high.	B
IN+	3	OUT stuck low	B
OUT	4	Posiible OUT pin and driver damge.	A
VDD	5	VDD and GND short circuit. No power is applied to the device.	D

Table 4-4. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No power is applied to the device.	D
GND	2	OUT is pulled up to VDD level.	B
IN+	3	OUT stuck low.	B
IN-	4	OUT stuck low.	B
OUT	5	OUT operates normally. Connection to the gate of Power FET is lost.	B

Table 4-5. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	UCC27518A-Q1 UCC27519A-Q1Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	OUT is enabled	B
GND	2	OUT stuck high.	B
IN-	3	OUT stuck low.	B
IN+	3	OUT stuck low.	B
OUT	4	OUT is floating	B
VDD	5	No power is applied to the device.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	GND	VDD and GND short circuit. No power is applied to the device.	D
GND	2	IN+	OUT stuck low.	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	UCC27518A-Q1 UCC27519A-Q1 Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	GND	OUT is disabled	B
GND	2	IN-	OUT stuck high.	B
GND	2	IN+	OUT stuck low.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Short to same potential. No impact.	D
GND	2	VDD and GND short circuit. No power is applied to the device.	D
IN+	3	OUT stuck high if IN- is low.	B
IN-	4	OUT stuck low.	B
OUT	5	Possible OUT pin and driver damge.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	UCC27518A-Q1 UCC27519A-Q1Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	OUT is enabled. EN is stuck high.	B
GND	2	VDD and GND short circuit. No power is applied to the device.	D
IN-	3	OUT stuck low.	B
IN+	3	OUT stuck high.	B
OUT	4	Possible OUT pin and driver damge.	A
VDD	5	Short to same potential. No impact.	D

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