Functional Safety Information

REF20-Q1

Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for REF20-Q1 (DDC package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

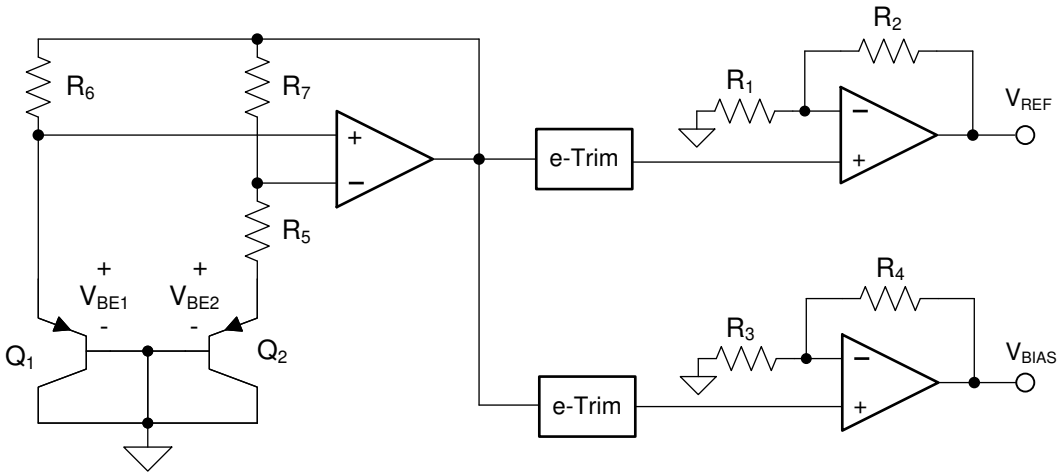

Figure 1-1. Functional Block Diagram

REF20-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for REF20-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

TABLE	CATEGORY	REFERENCE FIT RATE	REFERENCE VIRTUAL T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for REF20-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

DIE FAILURE MODES	FAILURE MODE DISTRIBUTION (%)
Output is stuck (high or low)	20 %
Output is floating	20 %
Incorrect output voltage	20 %
Supply current higher than specification	15 %
Incorrect start-up time	10 %
Oscillations at output	10 %
Temperature coefficient violates specification	5 %

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the REF20-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

CLASS	FAILURE EFFECTS
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the REF20-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the REF20-Q1data sheet.

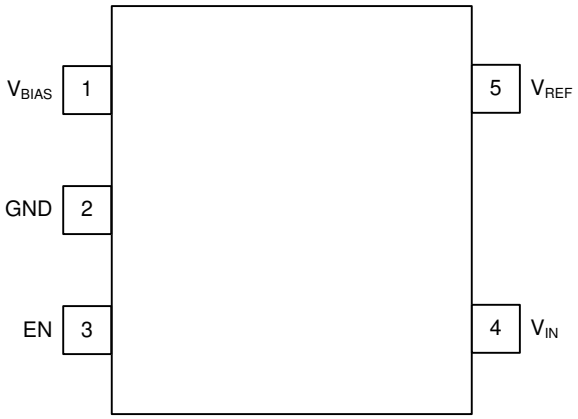

Figure 4-1. Pin Diagram

Unless otherwise specified, it is assumed that the voltages applied to all the pins are within the Recommended Operating Range specified in the datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
V_{BIAS}	1	Might damage the device, can affect functionality. Forces short circuit current to flow through device.	A
GND	2	Normal operation.	D
EN	3	No device damage. Device output will be disabled. System current may increase.	B
V_{IN}	4	No device damage. Device will not generate output. Increased system current.	B
V_{REF}	5	Might damage the device, can affect functionality. Forces short circuit current to flow through device.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
V_{BIAS}	1	No bias output voltage.	B
GND	2	No output voltage.	B
EN	3	No damage to device, can affect functionality.	B
V_{IN}	4	Device is unpowered.	B
V_{REF}	5	No reference output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

PIN NAME	PIN NO.	SHORTED TO	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
V_{BIAS}	1	GND	Might damage the device, can affect functionality. Forces short circuit current to flow through device.	A
GND	2	EN	No device damage. Device output will be disabled.	B
EN	3	V_{IN}	No damage to device. Device disable functionality will be lost. System current may increase.	B
V_{IN}	4	V_{REF}	Might damage the device. High current flow into the reference output.	A
V_{REF}	5	V_{BIAS}	Might damage the device. High current will flow from reference output to bias output.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN Supply

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
V_{BIAS}	1	Might damage the device. High current flow into the bias output.	A
GND	2	No device damage. Device will not generate output. Increased system current.	B
EN	3	No damage to device. Device disable functionality will be lost. System current may increase.	B
V_{IN}	4	Normal operation.	D
V_{REF}	5	Might damage the device. High current flow into the bias output.	A

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