Functional Safety Information

ADS1x7Lx1x Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the ADS117L11 (WQFN package), ADS127L11 (TSSOP and WQFN packages), ADS127L21 (WQFN package), and ADS127L21B (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

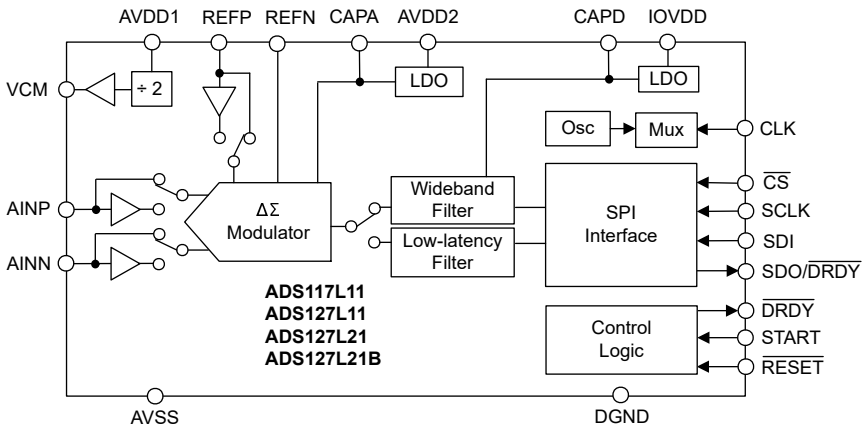

Figure 1-1. Functional Block Diagram

The ADS117L11, ADS127L11, ADS127L21, and ADS127L21B were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 TSSOP Package

This section provides functional safety failure in time (FIT) rates for the TSSOP package of the ADS127L11 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	2
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 18.5mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 WQFN Package

This section provides functional safety failure in time (FIT) rates for the WQFN package of the ADS117L11, ADS127L11, ADS127L21 and the ADS127L21B based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	2
Package FIT rate	6

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 18.5mW (33mW for ADS127L21)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ADS117L11, ADS127L11, ADS127L21, and ADS127L21B in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Analog input stuck at	20
Digital control pins stuck at	20
Output code bit stuck at	10
Communication error	10
10x input leakage current	10
10% shift of gain or offset	20
Oscillator frequency exceeds specification	5
VCM pin voltage exceeds specification	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ADS117L11 (WQFN package), ADS127L11 (TSSOP and WQFN packages), ADS127L21 (WQFN package), and ADS127L21B (WQFN package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD1 = AVDD2 = IOVDD = 5V
- AVSS = Thermal pad voltage = 0V
- IOVDD power-supply voltage is the same supply voltage used for driving the digital inputs
- *Short-circuit to supply* means short to AVDD1 = AVDD2 = IOVDD
- *Short-circuit to ground* means short to DGND = AVSS
- The VCM output voltage is actively used in the external circuit to establish the input common-mode voltage
- The device is the only peripheral device on the SPI bus
- Series resistors are used on the analog inputs and are sized to limit the input currents into the analog inputs to <10mA in all circumstances, such as if the device is not powered with an input signal applied

4.1 TSSOP Package

Figure 4-1 shows the ADS127L11 pin diagram for the TSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ADS127L11 data sheet.

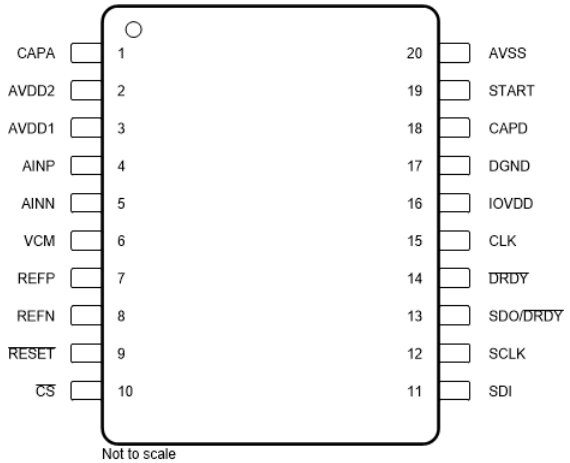

Figure 4-1. TSSOP Package Pin Diagram

Table 4-2. PW Package Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CAPA	1	The device is partially not powered and not functional. Device damage is plausible if CAPA is shorted to ground for an extended period of time.	A
AVDD2	2	The device is not powered and not functional.	B
AVDD1	3	The device is not powered and not functional. Observe that the absolute maximum ratings for the analog input and reference voltage pins of the device are met, otherwise device damage is plausible.	A
AINP	4	AINP is stuck low. Conversion results are correct only if AINP is tied to DGND in actual use, otherwise conversion results are incorrect.	B
AINN	5	AINN is stuck low. Conversion results are correct only if AINN is tied to DGND in actual use, otherwise conversions results are incorrect.	B
VCM	6	VCM is stuck low. Conversion results are incorrect if actively used for the external driver stage to set the signal common-mode voltage.	B
REFP	7	REFP is stuck low. Conversion results are incorrect.	B
REFN	8	REFN is stuck low. Conversion data are correct only if REFN is tied to DGND in actual use, otherwise conversion results are incorrect.	B
$\overline{\text{RESET}}$	9	$\overline{\text{RESET}}$ is stuck low. The device is not functional.	B
$\overline{\text{CS}}$	10	$\overline{\text{CS}}$ is stuck low in four-wire SPI mode. SPI communication is not functional because of the inability to control the SPI data frames.	B
		$\overline{\text{CS}}$ is stuck low in three-wire SPI mode. No effect, conversion results are correct.	D
SDI	11	SDI is stuck low. Loss of SPI input communication to the device. Conversion data readout remains functional.	B
SCLK	12	SCLK is stuck low. SPI communication is not possible.	B
SDO/$\overline{\text{DRDY}}$	13	SDO/$\overline{\text{DRDY}}$ is stuck low. SPI *output* communication is not possible. SPI input communication remains functional. The data-ready function with this pin is not functional. Device damage is plausible if SDO/$\overline{\text{DRDY}}$ is shorted to ground for an extended period of time.	A
$\overline{\text{DRDY}}$	14	$\overline{\text{DRDY}}$ is stuck low, this pin *is not* monitored by the host. Normal operation. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to ground for an extended period of time.	A
		$\overline{\text{DRDY}}$ is stuck low, this pin *is* monitored by the host. No data-ready indication with $\overline{\text{DRDY}}$ to the host is possible. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to ground an for extended period of time.	A
CLK	15	CLK is stuck low in *external* clock mode. The device is not functional. Conversion results are incorrect.	B
		CLK is stuck low in *internal* clock mode. No effect. Normal operation.	D
IOVDD	16	The device is not powered and not functional.	B
DGND	17	No effect. Normal operation.	D
CAPD	18	The device is partially not powered and not functional. Device damage is plausible if CAPD is shorted to ground for an extended period of time.	A
START	19	START is stuck low, this pin is in active use by the host. Loss of ability to control conversion timing. Conversion results are incorrect.	B
		START is stuck low, this pin is tied low in actual use (software control mode). No effect. Normal operation.	D
AVSS	20	No effect. Normal operation.	D

Table 4-3. PW Package Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CAPA	1	CAPA voltage is indeterminate. Conversion results are indeterminate.	B
AVDD2	2	The device is partially not powered and held in reset. The device is not functional.	B
AVDD1	3	Device functionality is indeterminate. The device is partially not powered and not functional if the analog input or voltage reference pins are held low. The device can be powered through input or voltage reference drivers through an internal ESD diode conduction path.	B
AINP	4	State of AINP is indeterminate. Conversion results are indeterminate.	B
AINN	5	State of AINN is indeterminate. Conversion results are indeterminate.	B
VCM	6	VCM output voltage is indeterminate. Conversion results are indeterminate.	B
REFP	7	State of REFP is indeterminate. Conversion results are indeterminate.	B
REFN	8	State of REFN is indeterminate. Conversion results are indeterminate.	B
$\overline{\text{RESET}}$	9	$\overline{\text{RESET}}$ is stuck high. Loss of ability to reset the ADC with this pin.	B
$\overline{\text{CS}}$	10	State of $\overline{\text{CS}}$ is indeterminate. SPI communication is corrupted.	B
SDI	11	State of SDI is indeterminate. Loss of SPI *input* communication to the device. Conversion data readout remains functional.	B
SCLK	12	State of SCLK is indeterminate. SPI communication is corrupted.	B
SDO/$\overline{\text{DRDY}}$	13	State of SDO/$\overline{\text{DRDY}}$ is indeterminate. SPI *output* communication is not possible. SPI input communication remains functional. Loss of data-ready function from this pin.	B
$\overline{\text{DRDY}}$	14	$\overline{\text{DRDY}}$ unconnected, this pin *is not* monitored by the host. No effect. Normal operation.	D
		$\overline{\text{DRDY}}$ unconnected, this pin *is* monitored by the host. No data-ready indication with $\overline{\text{DRDY}}$ to the host is possible.	B
CLK	15	CLK open-circuit in *external* clock mode. The device is not functional. Conversion results are incorrect.	B
		CLK open-circuit in *internal* clock mode. No effect. Normal operation.	D
IOVDD	16	Device functionality is indeterminate. The device is partially not powered and not functional if the START digital input pin is held low. The device can be powered through the START digital input pin with an internal ESD diode conduction path to IOVDD.	B
DGND	17	Device functionality is indeterminate. The device can be not powered, or powered through digital inputs with an ESD diode path.	B
CAPD	18	CAPD voltage is indeterminate. Conversion results are indeterminate.	B
START	19	State of START is indeterminate. Conversion results are indeterminate.	B
AVSS	20	Device functionality is indeterminate. The device is not powered and not functional if the analog input or voltage reference pins are held low. The device can be powered through the input or voltage reference drivers through an internal ESD diode conduction path.	B

Table 4-4. PW Package Pin FMA for Device Pins Short-Circuited to Adjacent Pins

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
CAPA	1	AVDD2	Device damage.	A
AVDD2	2	AVDD1	No effect. Normal operation.	D
AVDD1	3	AINP	Conversion results are correct only if AINP is tied to AVDD1 in actual use, otherwise conversion results are incorrect.	B
AINP	4	AINN	Conversion results are incorrect. Conversion result is close to 0V.	B
AINN	5	VCM	Conversion results are incorrect.	B
VCM	6	REFP	Conversion results are incorrect.	B
REFP	7	REFN	Conversion results are incorrect.	B
REFN	8	$\overline{\text{RESET}}$	Conversion results are incorrect. The device is held in reset and is not functional if the driver source impedance of REFN exceeds that of $\overline{\text{RESET}}$, thus driving $\overline{\text{RESET}}$ to a low threshold. Otherwise, conversion results are incorrect.	B
$\overline{\text{RESET}}$	9	$\overline{\text{CS}}$	Conversion results are incorrect. The device is not functional.	B
$\overline{\text{CS}}$	10	SDI	Not considered. Corner pins.	D
SDI	11	SCLK	Loss of SPI *input* communication to the device if the driver source impedance of SCLK exceeds that of SDI. Loss of *all* SPI communication to the device if the driver source impedance of SDI exceeds that of SCLK.	B
SCLK	12	SDO/$\overline{\text{DRDY}}$	Loss of SPI *output* communication from the device if the driver source impedance of SCLK exceeds that of SDO/$\overline{\text{DRDY}}$. Loss of *all* SPI communication to the device if the driver source impedance of SDO/$\overline{\text{DRDY}}$ exceeds that of SCLK. Device damage is plausible if shorted together for an extended period of time.	A
SDO/$\overline{\text{DRDY}}$	13	$\overline{\text{DRDY}}$	Indeterminate state of both digital outputs. Loss of SPI *output* communication from the device. Device damage is plausible if shorted together for an extended period of time.	A
$\overline{\text{DRDY}}$	14	CLK	*External* clock mode. The device is not functional if the driver source impedance of $\overline{\text{DRDY}}$ exceeds that of CLK. Indeterminate state of $\overline{\text{DRDY}}$ if the driver source impedance of CLK exceeds that of $\overline{\text{DRDY}}$. Device damage is plausible if shorted together for an extended period of time.	A
			Internal clock mode. The CLK pin has external pullup or pulldown resistor to supply or ground (no active driver used). Normal operation.	D
CLK	15	IOVDD	*External* clock mode. The device is not functional. Conversion results are incorrect.	B
			Internal clock mode. Normal operation.	D
IOVDD	16	DGND	The device is not powered and not functional.	B
DGND	17	CAPD	The device is partially not powered and not functional. Device damage is plausible if CAPD is shorted to ground for an extended period of time.	A
CAPD	18	START	The device is not functional. Permanent device damage if the START driver source impedance exceeds that of CAPD, resulting in CAPD exceeding the maximum voltage rating.	A
START	19	AVSS	Conversion results are correct only if START is tied to DGND = AVSS in actual use. Otherwise, conversion results are not correct because of inability to control conversions.	B
AVSS	20	CAPA	Not considered. Corner pins.	D

Table 4-5. PW Package Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CAPA	1	CAPA is stuck high. Permanent device damage.	A
AVDD2	2	No effect. Normal operation.	D
AVDD1	3	No effect. Normal operation.	D
AINP	4	AINP is stuck high. Conversion results are correct only if AINP is tied to AVDD1 in actual use, otherwise conversion results are incorrect.	B
AINN	5	AINN is stuck high. Conversion results are correct only if AINN is tied to AVDD1 in actual use, otherwise conversion results are incorrect.	B
VCM	6	VCM is stuck high. Conversion results are incorrect.	B
REFP	7	REFP is stuck high. Conversion results are correct only if REFP is tied to AVDD1 in actual use, otherwise conversion results are incorrect.	B
REFN	8	REFN is stuck high. Conversion results are incorrect.	B
$\overline{\text{RESET}}$	9	$\overline{\text{RESET}}$ is stuck high. Normal operation except for loss of $\overline{\text{RESET}}$ functionality.	B
$\overline{\text{CS}}$	10	$\overline{\text{CS}}$ is stuck high. SPI communication not functional.	B
SDI	11	SDI is stuck high. Loss of SPI input communication to the device. Conversion data readout remains functional.	B
SCLK	12	SCLK is stuck high. SPI communication is not possible.	B
SDO/$\overline{\text{DRDY}}$	13	SDO/$\overline{\text{DRDY}}$ is stuck high. SPI communication is not functional. Data ready not functional. Device damage is plausible if SDO/$\overline{\text{DRDY}}$ is shorted to the supply for an extended period of time.	A
$\overline{\text{DRDY}}$	14	$\overline{\text{DRDY}}$ is stuck high, this pin *is not* monitored. Normal operation. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to the supply for an extended period of time.	A
		$\overline{\text{DRDY}}$ is stuck high, this pin *is* monitored. No data-ready indication with $\overline{\text{DRDY}}$ to the host is possible. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to supply for an extended period of time.	A
CLK	15	CLK is stuck high in *external* clock mode. The device is not functional. Conversion results are incorrect.	B
		CLK is stuck high in *internal* clock mode. No effect. Normal operation.	D
IOVDD	16	No effect. Normal operation.	D
DGND	17	The device is not powered and not functional.	B
CAPD	18	CAPD is stuck high. Permanent device damage.	A
START	19	START is stuck high. Conversion results are correct only if START is tied to IOVDD in actual use. Otherwise, conversion results are incorrect because of the loss of ability to control conversions.	B
AVSS	20	The device is not powered and not functional.	B

4.2 WQFN Package

Figure 4-2 shows the ADS117L11, ADS127L11, ADS127L21, and ADS127L21B pin diagram for the WQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* sections in the ADS117L11, ADS127L11, ADS127L21, and ADS127L21B data sheets.

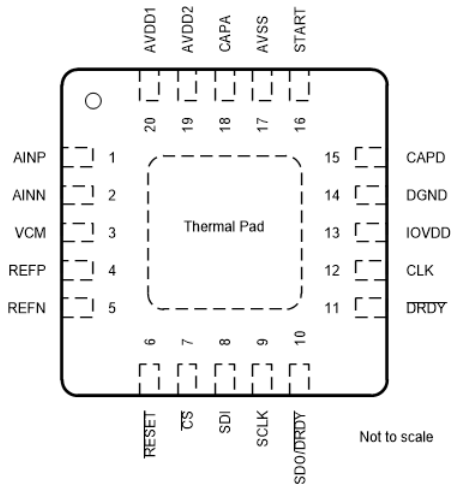

Figure 4-2. Pin Diagram (WQFN Package)

Table 4-6. RUK Package Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
AINP	1	AINP is stuck low. Conversion results are correct only if AINP is tied to DGND in actual use, otherwise conversion results are incorrect.	B
AINN	2	AINN is stuck low. Conversion results are correct only if AINN is tied to DGND in actual use, otherwise conversions results are incorrect.	B
VCM	3	VCM is stuck low. Conversion results are incorrect if actively used for the external driver stage to set the signal common-mode voltage.	B
REFP	4	REFP is stuck low. Conversion results are incorrect.	B
REFN	5	REFN is stuck low. Conversion data are correct only if REFN is tied to DGND in actual use, otherwise conversions results are incorrect.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ is stuck low. The device is not functional.	B
$\overline{\text{CS}}$	7	$\overline{\text{CS}}$ is stuck low in four-wire SPI mode. SPI communication is not functional because of inability to control SPI data frames.	B
		$\overline{\text{CS}}$ is stuck low in three-wire SPI mode. No effect, conversions results are correct.	D
SDI	8	SDI is stuck low. Loss of SPI input communications to the device. Conversion data readout remains functional.	B
SCLK	9	SCLK is stuck low. SPI communication is not possible.	B
SDO/$\overline{\text{DRDY}}$	10	SDO/$\overline{\text{DRDY}}$ is stuck low. SPI *output* communication is not possible. SPI input communication remains functional. The data-ready function with this pin is not functional. Device damage plausible if SDO/$\overline{\text{DRDY}}$ is shorted to ground for an extended period of time.	A
$\overline{\text{DRDY}}$	11	$\overline{\text{DRDY}}$ is stuck low, this pin *is not* monitored by the host. Normal operation. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to ground for an extended period of time.	A
		$\overline{\text{DRDY}}$ is stuck low, this pin *is* monitored by the host. No data-ready indication with $\overline{\text{DRDY}}$ to the host is possible. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to ground for an extended period of time.	A
CLK	12	CLK is stuck low in *external* clock mode. The device is not functional. Conversion results are incorrect.	B
		CLK is stuck low in *internal* clock mode. No effect. Normal operation.	D
IOVDD	13	The device is not powered and not functional.	B
DGND	14	No effect. Normal operation.	D
CAPD	15	The device is partially not powered and not functional. Device damage is plausible if CAPD is shorted to ground for an extended period of time.	A
START	16	START is stuck low, this pin is in active use by the host. Loss of ability to control conversion timing. Conversion results are incorrect.	B
		START is stuck low, this pin is tied low in actual use (software control mode). No effect. Normal operation.	D
AVSS	17	No effect. Normal operation.	D
CAPA	18	The device is partially not powered and is not functional. Device damage is plausible if CAPA is shorted to ground for an extended period of time.	A
AVDD2	19	The device is not powered and not functional.	B
AVDD1	20	The device is not powered and not functional. Observe that the absolute maximum ratings for the analog input and reference voltage pins of the device are met, otherwise device damage is plausible.	A
Thermal pad	—	No effect. Normal operation.	D

Table 4-7. RUK Package Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
AINP	1	State of AINP is indeterminate. Conversion results are indeterminate.	B
AINN	2	State of AINN is indeterminate. Conversion results are indeterminate.	B
VCM	3	VCM output voltage is indeterminate. Conversion results are indeterminate.	B
REFP	4	State of REFP is indeterminate. Conversion results are indeterminate.	B
REFN	5	State of REFN is indeterminate. Conversion results indeterminate.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ is stuck high. Loss of ability to reset the ADC with this pin.	B
$\overline{\text{CS}}$	7	State of $\overline{\text{CS}}$ is indeterminate. SPI communication is corrupted.	B
SDI	8	State of SDI is indeterminate. Loss of SPI *input* communication to the device. Conversion data readout remains functional.	B
SCLK	9	State of SCLK is indeterminate. SPI communication is corrupted.	B
SDO/$\overline{\text{DRDY}}$	10	State of SDO/$\overline{\text{DRDY}}$ is indeterminate. SPI *output* communication is not possible. SPI input communication remains functional. Loss of data-ready function from this pin.	B
$\overline{\text{DRDY}}$	11	$\overline{\text{DRDY}}$ is unconnected, this pin *is not* monitored by the host. No effect. Normal operation.	D
		$\overline{\text{DRDY}}$ is unconnected, this pin *is* monitored by the host. No data-ready indication with $\overline{\text{DRDY}}$ to the host is possible.	B
CLK	12	CLK is open circuit in *external* clock mode. The device is not functional. Conversion results are incorrect.	B
		CLK is open circuit in *internal* clock mode. No effect. Normal operation.	D
IOVDD	13	Device functionality is undetermined. The device is partially not powered and not functional if the START digital input pin is held low. The device can be powered through the START digital input pin by an internal ESD diode conduction path to IOVDD.	B
DGND	14	Device functionality is indeterminate. The device can be not powered, or powered through digital inputs by an ESD diode path.	B
CAPD	15	CAPD voltage is indeterminate. Conversion results are indeterminate.	B
START	16	State of START is indeterminate. Conversion results are indeterminate.	B
AVSS	17	Device functionality is indeterminate. The device is not powered and not functional if the analog input or voltage reference pins are held low. The device can be powered through input or voltage reference drivers through an internal ESD diode conduction path.	B
CAPA	18	CAPA voltage is indeterminate. Conversion results are indeterminate.	B
AVDD2	19	The device is partially not powered and held in reset. The device is not functional.	B
AVDD1	20	Device functionality is indeterminate. The device is partially not powered and not functional if the analog input or voltage reference pins are held low. The device can be powered through input or voltage reference drivers through an internal ESD diode conduction path.	B
Thermal pad	—	The device remains functional with possible performance degradation.	C

Table 4-8. RUK Package Pin FMA for Device Pins Short-Circuited to Adjacent Pins

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
AINP	1	AINN	Conversion results are incorrect. Conversion result is close to 0V.	B
AINN	2	VCM	Conversion results are incorrect.	B
VCM	3	REFP	Conversion results are incorrect.	B
REFP	4	REFN	Conversion results are incorrect.	B
REFN	5	$\overline{\text{RESET}}$	Not considered. Corner pins.	D
$\overline{\text{RESET}}$	6	$\overline{\text{CS}}$	Conversion results are incorrect. The device is not functional.	B
$\overline{\text{CS}}$	7	SDI	Loss of SPI *input* communication to the device if the driver source impedance of $\overline{\text{CS}}$ exceeds that of SDI. Loss of *all* SPI communication to the device if the driver source impedance of SDI exceeds that of $\overline{\text{CS}}$.	B
SDI	8	SCLK	Loss of SPI *input* communication to the device if the driver source impedance of SCLK exceeds that of SDI. Loss of *all* SPI communication to the device if the driver source impedance of SDI exceeds that of SCLK.	B
SCLK	9	SDO/$\overline{\text{DRDY}}$	Loss of SPI *output* communication from the device if the driver source impedance of SCLK exceeds that of SDO/$\overline{\text{DRDY}}$. Loss of *all* SPI communication to the device if the driver source impedance of SDO/$\overline{\text{DRDY}}$ exceeds that of SCLK. Device damage is plausible if shorted together for an extended period of time.	A
SDO/$\overline{\text{DRDY}}$	10	$\overline{\text{DRDY}}$	Not considered. Corner pins.	D
$\overline{\text{DRDY}}$	11	CLK	*External* clock mode. The device is not functional if the driver source impedance of $\overline{\text{DRDY}}$ exceeds that of CLK. Indeterminate state of $\overline{\text{DRDY}}$ if the driver source impedance of CLK exceeds that of $\overline{\text{DRDY}}$. Device damage is plausible if shorted together for an extended period of time.	A
			Internal clock mode. The CLK pin has an external pullup or pulldown resistor to supply or ground (no active driver used). Normal operation.	D
CLK	12	IOVDD	*External* clock mode. The device is not functional. Conversion results are incorrect.	B
			Internal clock mode. Normal operation.	D
IOVDD	13	DGND	The device is partially not powered and not functional.	B
DGND	14	CAPD	The device is partially not powered and not functional. Device damage is plausible if CAPD is shorted to ground for an extended period of time.	A
CAPD	15	START	Not considered. Corner pins.	D
START	16	AVSS	Conversion results are correct only if START is tied to DGND = AVSS in actual use. Otherwise, conversion results are not correct because of the inability to control conversions.	B
AVSS	17	CAPA	The device is partially not powered and not functional.	B
CAPA	18	AVDD2	CAPA is stuck high. Permanent device damage.	A
AVDD2	19	AVDD1	No effect. Normal operation.	D
AVDD1	20	AINP	Not considered. Corner pins.	D
Thermal pad	—	All pins	See the device pins short circuited to ground table (Table 4-6).	-

Table 4-9. RUK Package Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
AINP	1	AINP is stuck high. Conversion results are correct only if AINP is tied to AVDD1 in actual use, otherwise conversion results are incorrect.	B
AINN	2	AINN is stuck high. Conversion results are correct only if AINN is tied to AVDD1 in actual use, otherwise conversion results are incorrect.	B
VCM	3	VCM is stuck high. Conversion results are incorrect.	B
REFP	4	REFP is stuck high. Conversion results correct only if REFP is tied to AVDD1 in actual use, otherwise conversions results incorrect.	B
REFN	5	REFN is stuck high. Conversion results are incorrect.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ is stuck high. Normal operation except for the loss of $\overline{\text{RESET}}$ functionality.	B
$\overline{\text{CS}}$	7	$\overline{\text{CS}}$ is stuck high. SPI communication is not functional.	B
SDI	8	SDI is stuck high. Loss of SPI input communication to the device. Conversion data readout remains functional.	B
SCLK	9	SCLK is stuck high. SPI communication is not possible.	B
SDO/$\overline{\text{DRDY}}$	10	SDO/$\overline{\text{DRDY}}$ is stuck high. SPI communication is not functional. Data ready is not functional. Device damage is plausible if SDO/$\overline{\text{DRDY}}$ is shorted to the supply for an extended period of time.	A
$\overline{\text{DRDY}}$	11	$\overline{\text{DRDY}}$ is stuck high, this pin *is not* monitored. Normal operation. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to the supply for an extended period of time.	A
		$\overline{\text{DRDY}}$ is stuck high, this pin *is* monitored. No data-ready indication by $\overline{\text{DRDY}}$ to the host is possible. Device damage is plausible if $\overline{\text{DRDY}}$ is shorted to the supply for an extended period of time.	A
CLK	12	CLK is stuck high in *external* clock mode. The device is not functional. Conversion results are incorrect.	B
		CLK is stuck high in *internal* clock mode. No effect. Normal operation.	D
IOVDD	13	No effect. Normal operation.	D
DGND	14	The device is not powered and not functional.	B
CAPD	15	CAPD is stuck high. Permanent device damage.	A
START	16	START is stuck high. Conversion results are correct only if START is tied to 5V in actual use. Otherwise, conversion results are incorrect because of loss of ability to control conversions.	B
AVSS	17	The device is not powered and not functional.	B
CAPA	18	CAPA is stuck high. Permanent device damage.	A
AVDD2	19	No effect. Normal operation.	D
AVDD1	20	No effect. Normal operation.	D
Thermal pad	—	The device is not powered and not functional.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2023) to Revision C (September 2024)	Page
• Added ADS127L21B to document	2

Changes from Revision A (January 2023) to Revision B (July 2023)	Page
• Added ADS127L21 to document	2

Changes from Revision * (September 2021) to Revision A (January 2023)	Page
• Added ADS117L11 to document	2

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