Functional Safety Information

UCC12051-Q1 , UCC12041-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for UCC12051-Q1 and UCC12041-Q1 (DVE SOIC (16) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

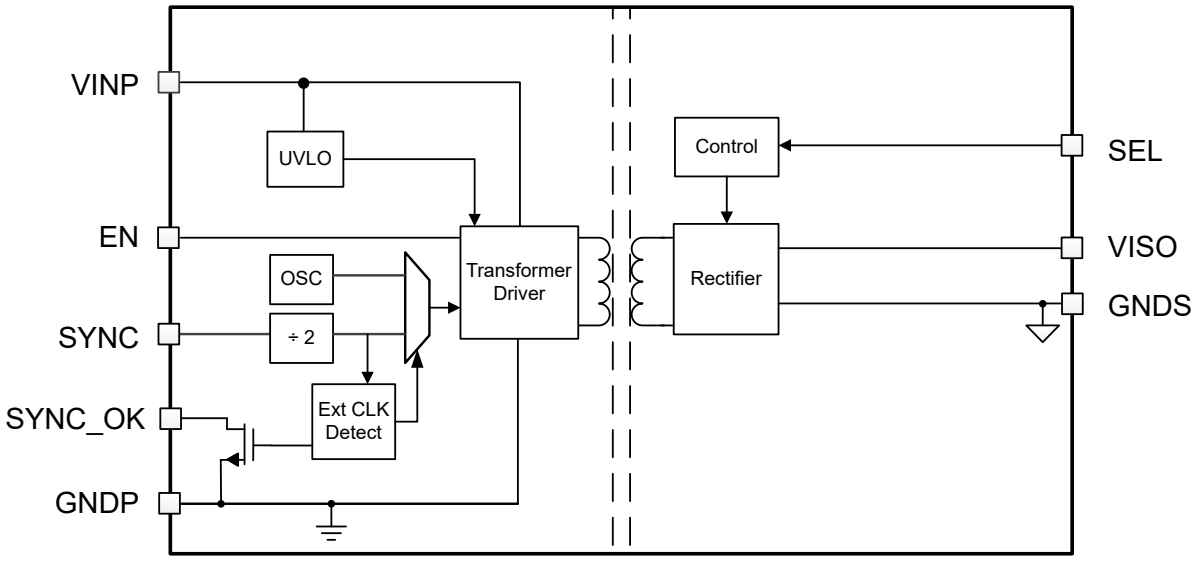

Figure 1-1. Functional Block Diagram

UCC12051-Q1 and UCC12041-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC12051-Q1 and UCC12041-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (400 mW, 200 mW, 100 mW)	30, 28, 26
Die FIT Rate (400 mW, 200 mW, 100 mW)	4, 3, 2
Package FIT Rate (400 mW, 200 mW, 100 mW)	26, 25, 24

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 400 mW, 200 mW, 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC12051-Q1 and UCC12041-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output	61
Incorrect output regulation	25
No effect	14

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC12051-Q1 and UCC12041-Q1 . The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC12051-Q1 and UCC12041-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC12051-Q1 and UCC12041-Q1 data sheet.

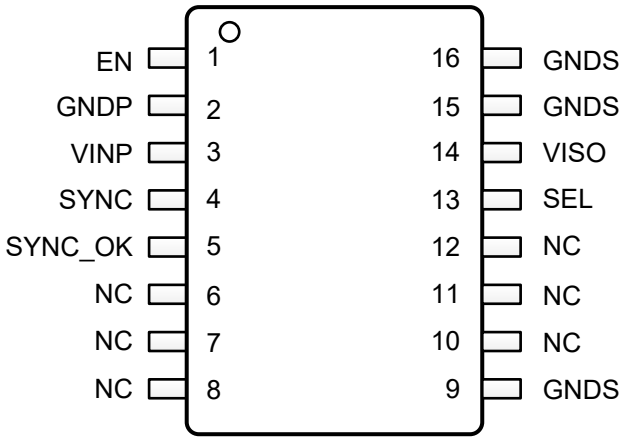

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pull-down resistor on SYNC to GNDP
- External pull-up resistor on SYNC_OK to VINP
- EN connected to VINP
- NC pins 6-8 are connected to GNDP
- SEL connected to VISO (5 VISO)
- NC pins 10-12 are connected to GNDS
- GNDP is considered as the Ground for pin 1 through 8
- GNDS is considered as the Ground for pin 9 through 16
- VINP is considered as the supply for pin 1 through 8
- VISO is considered as the supply for pin 9 through 16

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)[1][2]	Failure Effect Class
EN	1	Disabled state, VISO remains off (~ 0 V)	B
GNDP	2	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
VINP	3	Will short externally provided VINP supply. Non-functional, no supply, VISO remains off (~ 0 V)	B
SYNC	4	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
SYNC_OK	5	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	6	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	7	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	8	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
GNDS	9	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	10	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	11	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	12	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
SEL	13	Short SEL and VISO output to ground (~ 0 V, non-functional)	B
VISO	14	Short VISO and SEL output to ground (~ 0 V, non-functional)	B
GNDS	15	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
GNDS	16	Normal functionality, VISO regulates to the programmed value set by SEL pin	D

(1) GNDP is considered as the Ground for pin 1 through 8
(2) GNDS is considered as the Ground for pin 9 through 16

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	Disabled state, VISO remains off (~ 0 V). 100-kΩ internal pull-down	B
GNDP	2	No VISO output	B
VINP	3	Non-functional, no supply path, VISO remains off (~ 0 V)	B
SYNC	4	Possible noise coupling leading to corruption of the internal oscillator. May result in an incorrectly regulated VISO DC value, unstable output, or inability to maintain VISO load line performance	C
SYNC_OK	5	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	6	No impact	D
NC	7	No impact	D
NC	8	No impact	D
GNDS	9	Normal functionality, VISO regulates to the programmed value set by SEL pin. Less than ideal grounding (through leadframe and pins 10, 11, 12, and15)	D
NC	10	No impact	D
NC	11	No impact	D
NC	12	No impact	D
SEL	13	Unsupported VISO selection state - VISO will most likely regulate to 3.7 V due to internal high impedance pull-down, but results may vary due to floating state	C
VISO	14	VISO output may go unstable due to absence of output cap (may not regulate as expected)	C
GNDS	15	Normal functionality, VISO regulates to the programmed value set by SEL pin. Less than ideal grounding (through leadframe and pin 9), may see increased ripple on VISO output due to additional ground noise	D
GNDS	16	Normal functionality, VISO regulates to the programmed value set by SEL pin	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	GNDP	Disabled state, VISO remains off (~ 0 V)	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GNDP	2	VINP	Will short externally provided VINP supply; Non-functional, no supply, VISO remains off (~ 0 V)	B
VINP	3	SYNC	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
SYNC	4	SYNC_OK	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
SYNC_OK	5	NC	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
NC	6	NC	No impact	D
NC	7	NC	No impact	D
NC	8	N/A	N/A	D
GNDS	9	NC	No impact	D
NC	10	NC	No impact	D
NC	11	NC	No impact	D
NC	12	SEL	SEL is connected to VISO. SEL shorted to NC means VISO shorted to GNDS, VISO is ~ 0 V, non-functional.	B
SEL	13	VISO	Normal functionality, VISO regulates to 5 V	D
VISO	14	GNDS	Will short VISO output to ground (VISO is ~ 0 V, non-functional),	B
GNDS	15	GNDS	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
GNDS	16	N/A	N/A	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)[1] [2]	Failure Effect Class
EN	1	Normal functional, VISO regulates to the programmed value set by SEL pin	D
GNDP	2	Will short to externally provided VINP supply. Non-functional, no supply, VISO remains off (~ 0 V)	B
VINP	3	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
SYNC	4	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
SYNC_OK	5	Potential overstress/damage of open-drain device if external clock on SYNC is ignored/not used (pin is actively pulled low internally). VISO will still regulate to the programmed value set by SEL pin.	A
NC	6	Will short to externally provided VINP supply. Non-functional, no supply, VISO remains off (~ 0 V)	B
NC	7	Will short to externally provided VINP supply. Non-functional, no supply, VISO remains off (~ 0 V)	B
NC	8	Will short to externally provided VINP supply. Non-functional, no supply, VISO remains off (~ 0 V)	B
GNDS	9	Will short VISO to ground (~ 0 V, non-functional)	B
NC	10	Will short VISO to ground (~ 0 V, non-functional)	B
NC	11	Will short VISO to ground (~ 0 V, non-functional)	B
NC	12	Will short VISO to ground (~ 0 V, non-functional)	B
SEL	13	Normal functionality, VISO regulates to 5V	D
VISO	14	Normal functionality, VISO regulates to the programmed value set by SEL pin	D
GNDS	15	Will short VISO to ground (~ 0 V, non-functional)	B
GNDS	16	Will short VISO to ground (~ 0 V, non-functional)	B

(1) VINP is considered as the supply for pin 1 through 8
(2) VISO is considered as the supply for pin 9 through 16

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