Functional Safety Information

CDCE6214-Q1
Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for CDCE6214-Q1 (VQFN-24 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

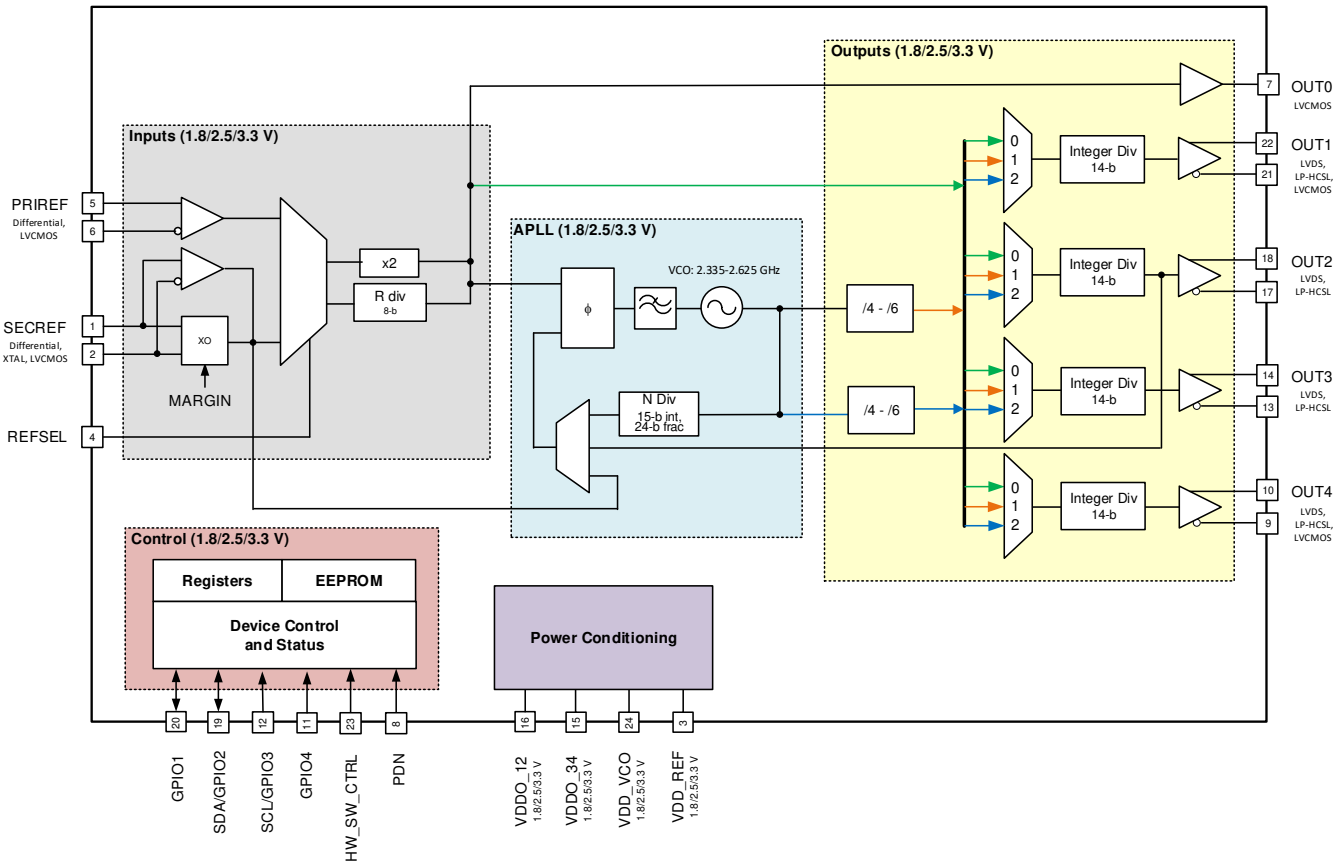

Figure 1-1. Functional Block Diagram

CDCE6214-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for CDCE6214-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	14
Die FIT Rate	3
Package FIT Rate	11

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 297 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =<50V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for CDCE6214-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Performance degradation of output clocks	45%
Incorrect output frequencies, poor timing accuracy	40%
Part in undefined state due to incorrect startup/power-on reset	15%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the CDCE6214-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-3)
- Pin open-circuited (see Table 4-4)
- Pin short-circuited to an adjacent pin (see Table 4-5)
- Pin short-circuited to supply (see Table 4-6)

In addition to the above mentioned pin-by-pin failure scenarios, Table 4-2 describes the assumptions that were made to determine the failure modes.

Table 4-3 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the CDCE6214-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the CDCE6214-Q1 data sheet.

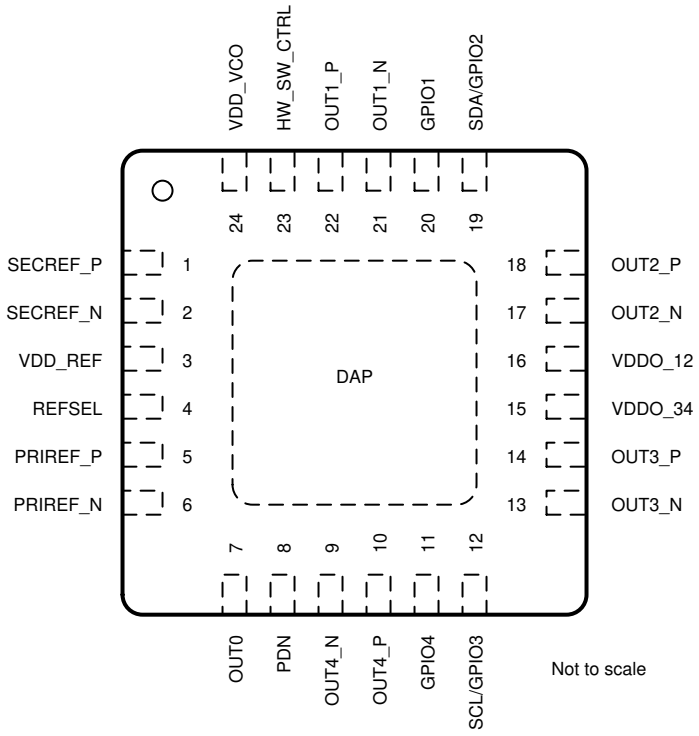

Figure 4-1. Pin Diagram

Table 4-2. Connection Assumptions for Device Pins

Pin Name	Pin No.	Assumptions
SECREF_P	1	Connected to output pins of device driving CDCE6214-Q1. Can be AC-coupled, or be connected to ground if CDCE6214-Q1 is driven single-ended.
SECREF_N	2	Connected to output pins of device driving CDCE6214-Q1. Can be AC-coupled, or be connected to ground if CDCE6214-Q1 is driven single-ended.
VDD_REF	3	Connected to power rail
REFSEL	4	Pulled up to power rail via 5-kΩ resistor, pulled down to ground via 5-kΩ resistor or left floating.
PRIREF_P	5	Connected to output pins of device driving CDCE6214-Q1. Can be AC-coupled, or be connected to ground if CDCE6214-Q1 is driven single-ended.
PRIREF_N	6	Connected to output pins of device driving CDCE6214-Q1. Can be AC-coupled, or be connected to ground if CDCE6214-Q1 is driven single-ended.
OUT0	7	Goes to input of the device CDCE6214-Q1 is driving
PDN	8	Connected to a 0.1-µF capacitor to ground
OUT4_N	9	Goes to input of the device CDCE6214-Q1 is driving
OUT4_P	10	Goes to input of the device CDCE6214-Q1 is driving
GPIO4	11	Pulled up to power rail via 5-kΩ resistor, pulled down to ground via 5-kΩ resistor or left floating.
SCL/GPIO3	12	Pulled-up to power rail via 5-kΩ, assuming I2C operation
OUT3_N	13	Goes to input of the device CDCE6214-Q1 is driving
OUT3_P	14	Goes to input of the device CDCE6214-Q1 is driving
VDDO_34	15	Connected to power rail
VDDO_12	16	Connected to power rail
OUT2_N	17	Goes to input of the device CDCE6214-Q1 is driving
OUT2_P	18	Goes to input of the device CDCE6214-Q1 is driving
SDA/GPIO2	19	Pulled-up to power rail via 5-kΩ, assuming I2C operation
GPIO1	20	Pulled up to power rail via 5-kΩ resistor, pulled down to ground via 5-kΩ resistor or left floating.
OUT1_N	21	Goes to input of the device CDCE6214-Q1 is driving
OUT1_P	22	Goes to input of the device CDCE6214-Q1 is driving
HW_SW_CTRL	23	Pulled up to power rail via 5-kΩ resistor, pulled down to ground via 5-kΩ resistor or left floating.
VDD_VCO	24	Connected to power rail
DAP	25	Connected to ground

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SECREF_P	1	Invalid input clock, PLL doesn't lock, no output clocks	B
SECREF_N	2	Invalid input clock, PLL doesn't lock, no output clocks	B
VDD_REF	3	Power-ground short can damage the device	A
REFSEL	4	Incorrect clock input may be selected, PLL doesn't lock, no output clocks	B
PRIREF_P	5	Invalid input clock, PLL doesn't lock, no output clocks	B
PRIREF_N	6	Invalid input clock, PLL doesn't lock, no output clocks	B
OUT0	7	Invalid output clock	B
PDN	8	Device stays in powerdown mode, no output clocks	B
OUT4_N	9	Invalid output clock	B

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT4_P	10	Invalid output clock	B
GPIO4	11	Unintended input or incorrect output forced	B
SCL/GPIO3	12	No I2C communication possible	B
OUT3_N	13	Invalid output clock	B
OUT3_P	14	Invalid output clock	B
VDDO_34	15	Power-ground short can damage the device	A
VDDO_12	16	Power-ground short can damage the device	A
OUT2_N	17	Invalid output clock	B
OUT2_P	18	Invalid output clock	B
SDA/GPIO2	19	No I2C communication possible	B
GPIO1	20	Unintended input or incorrect output forced	B
OUT1_N	21	Invalid output clock	B
OUT1_P	22	Invalid output clock	B
HW_SW_CTRL	23	Unintended input, device may start up in an incorrect state, PLL doesn’t lock, no output clocks	B
VDD_VCO	24	Power-ground short can damage the device	A
DAP	25	No damage	D

Table 4-4. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SECREF_P	1	Invalid input clock, PLL doesn't lock, no output clocks	B
SECREF_N	2	Invalid input clock, PLL doesn't lock, no output clocks	B
VDD_REF	3	No power to reference input and digital blocks of circuit, PLL doesn't lock, no output clocks, no I2C communication possible. Providing input signals violates absolute maximum ratings and can cause damage to device.	A
REFSEL	4	Incorrect clock input may be selected, PLL doesn't lock, no output clocks	B
PRIREF_P	5	Invalid input clock, PLL doesn't lock, no output clocks	B
PRIREF_N	6	Invalid input clock, PLL doesn't lock, no output clocks	B
OUT0	7	Invalid output clock	B
PDN	8	Pulled high via internal weak pull-up, device is functional.	D
OUT4_N	9	Invalid output clock	B
OUT4_P	10	Invalid output clock	B
GPIO4	11	Unintended input or incorrect output forced	B
SCL/GPIO3	12	No I2C communication possible	B
OUT3_N	13	Invalid output clock	B
OUT3_P	14	Invalid output clock	B
VDDO_34	15	No power to OUT0, OUT3, and OUT4 blocks of chip, no OUT0, OUT3 and OUT4 clocks present	B
VDDO_12	16	No power to OUT1 and OUT2 blocks of chip, no OUT1 and OUT2 clocks present	B
OUT2_N	17	Invalid output clock	B
OUT2_P	18	Invalid output clock	B

Table 4-4. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SDA/GPIO2	19	No I2C communication possible	B
GPIO1	20	Unintended input or incorrect output forced	B
OUT1_N	21	Invalid output clock	B
OUT1_P	22	Invalid output clock	B
HW_SW_CTRL	23	Unintended input, device may start up in an incorrect state, PLL doesn't lock, no output clocks	B
VDD_VCO	24	No power to OUT1 and OUT2 channels	B
DAP	25	Device not grounded, invalid power supplied to device Providing input signals violates absolute maximum ratings and can cause damage to device.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited With an Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potentitial Failure Effect(s)	Failure Effect Class
SECREF_P	1	SECREF_N	Invalid input clock, PLL doesn't lock, no output clocks	B
SECREF_N	2	VDD_REF	Invalid input clock, PLL doesn't lock, no output clocks	B
VDD_REF	3	REFSEL	Incorrect clock input may be selected, PLL doesn't lock, no output clocks	B
REFSEL	4	PRIREF_P	Incorrect clock input may be selected, PLL doesn't lock, no output clocks	B
PRIREF_P	5	PRIREF_N	Invalid input clock, PLL doesn't lock, no output clocks	B
PRIREF_N	6	OUT0	Invalid input clock, PLL doesn't lock, no output clocks	B
OUT0	7	PDN	Device may incorrectly enter/exit powerdown mode, no output clocks	B
PDN	8	OUT4_N	Device may incorrectly enter/exit powerdown mode, no output clocks	B
OUT4_N	9	OUT4_P	Invalid output clock	B
OUT4_P	10	GPIO4	Output clock present, voltage swing may be degraded	C
GPIO4	11	SCL/GPIO3	Possible interference with I2C communication	B
SCL/GPIO3	12	OUT3_N	Possible interference with I2C communication	B
OUT3_N	13	OUT3_P	Invalid output clock	B
OUT3_P	14	VDDO_34	Invalid output clock, could damage receiver device	B
VDDO_34	15	VDDO_12	No damage, possibly different output swing	C
VDDO_12	16	OUT2_N	Invalid output clock, could damage receiver device	B
OUT2_N	17	OUT2_P	Invalid output clock	B
OUT2_P	18	SDA/GPIO2	Possible interference with I2C communication	B
SDA/GPIO2	19	GPIO1	Possible interference with I2C communication	B

Table 4-5. Pin FMA for Device Pins Short-Circuited With an Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potentitial Failure Effect(s)	Failure Effect Class
GPIO1	20	OUT1_N	Output clock present, voltage swing may be degraded	C
OUT1_N	21	OUT1_P	Invalid output clock	B
OUT1_P	22	HW_SW_CTRL	Unintended input, device may start up in an incorrect state, PLL doesn't lock, no output clocks Alternatively, output clocks may be presented and OUT1 may have degraded voltage swing	B
HW_SW_CTRL	23	VDD_VCO	Unintended input, device may start up in an incorrect state, PLL doesn't lock, no output clocks	B
VDD_VCO	24	SECREF_P	Invalid input clock, PLL doesn't lock, no output clocks	B
DAP	25	Any pin	DAP is connect to ground, behavior will be the same as described in Table 4-3	N/A

Table 4-6. Pin FMA for Device Pins Short-Circuited to Power Rail

Pin Name	Pin No.	Description of Potentitial Failure Effect(s)	Failure Effect Class
SECREF_P	1	Invalid input clock, PLL doesn't lock, no output clocks	B
SECREF_N	2	Invalid input clock, PLL doesn't lock, no output clocks	B
VDD_REF	3	No damage, possibly different output swing	C
REFSEL	4	Incorrect clock input may be selected, PLL doesn't lock, no output clocks	B
PRIREF_P	5	Invalid input clock, PLL doesn't lock, no output clocks	B
PRIREF_N	6	Invalid input clock, PLL doesn't lock, no output clocks	B
OUT0	7	Invalid output clock, could damage receiver device	B
PDN	8	Device never enters powerdown, device is functional	D
OUT4_N	9	Invalid output clock, could damage receiver device	B
OUT4_P	10	Invalid output clock, could damage receiver device	B
GPIO4	11	Unintended input or incorrect output forced	B
SCL/GPIO3	12	No I2C communication possible	B
OUT3_N	13	Invalid output clock, could damage receiver device	B
OUT3_P	14	Invalid output clock, could damage receiver device	B
VDDO_34	15	No damage, possibly different output swing	C
VDDO_12	16	No damage, possibly different output swing	C
OUT2_N	17	Invalid output clock, could damage receiver device	B
OUT2_P	18	Invalid output clock, could damage receiver device	B
SDA/GPIO2	19	No I2C communication possible	B
GPIO1	20	Unintended input or incorrect output forced	B
OUT1_N	21	Invalid output clock, could damage receiver device	B
OUT1_P	22	Invalid output clock, could damage receiver device	B
HW_SW_CTRL	23	Unintended input, device may start up in an incorrect state, PLL doesn't lock, no output clocks	B
VDD_VCO	24	No damage, possibly different output swing	C
DAP	25	Power-ground short can damage the device	A

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