Functional Safety Information

DRV8872-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for DRV8872-Q1 to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

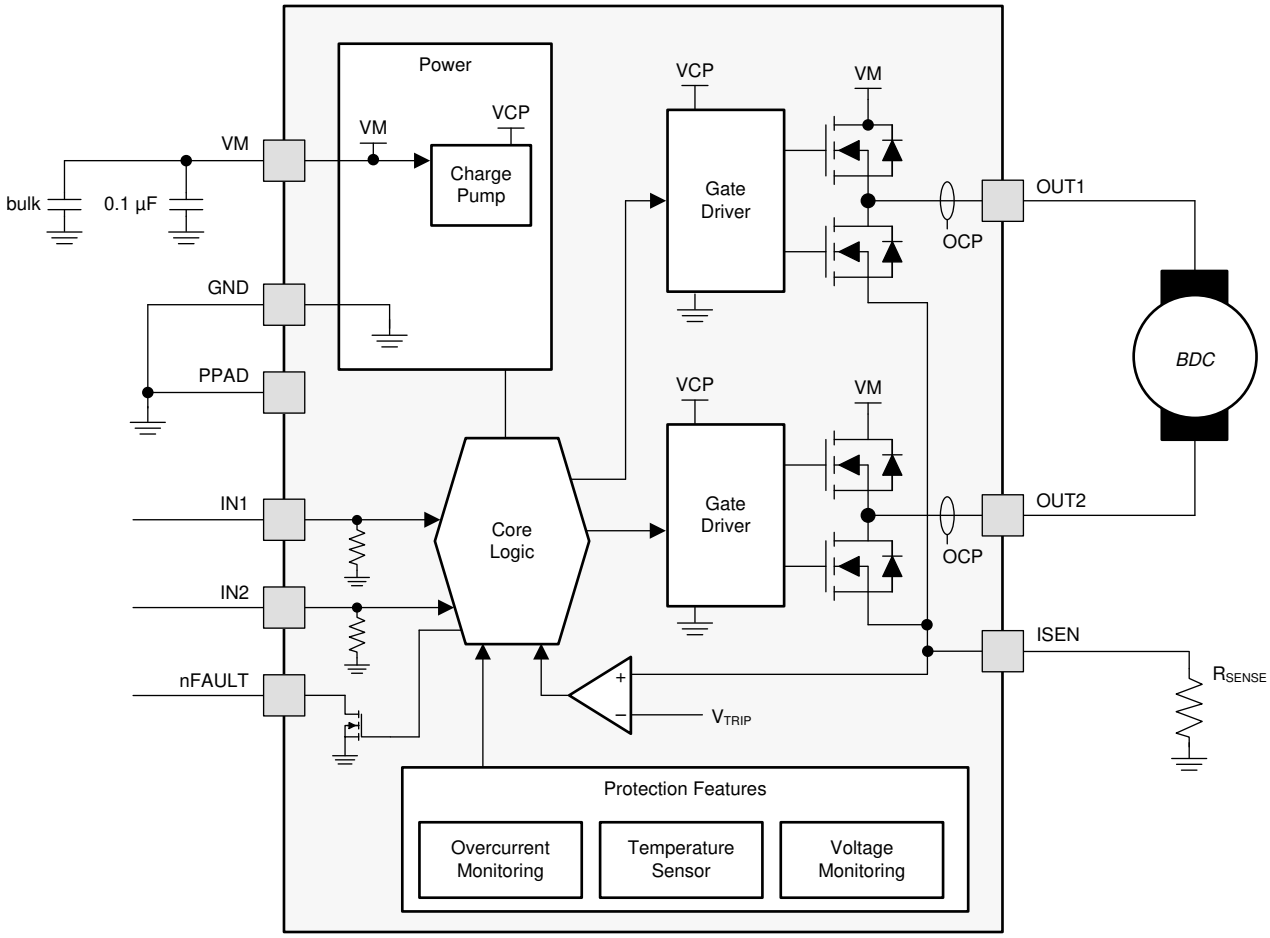

Figure 1-1. Functional Block Diagram

DRV8872-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8872-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	16
Die FIT Rate	8
Package FIT Rate	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 0.9 W
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8872-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTx is stuck low when commanded OFF	16%
OUTx is stuck OFF when commanded LOW	10%
OUTx ON resistance too high when commanded LOW	14%
OUTx is stuck HIGH when commanded OFF	16%
OUTx is stuck OFF when commanded HIGH	10%
OUTx ON resistance too high when commanded HIGH	19%
Dead-time is too short	1%
ITRIP current regulation incorrect	4%
Incorrect communication or fault indication	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the DRV8872-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the DRV8872-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the DRV8872-Q1 data sheet.

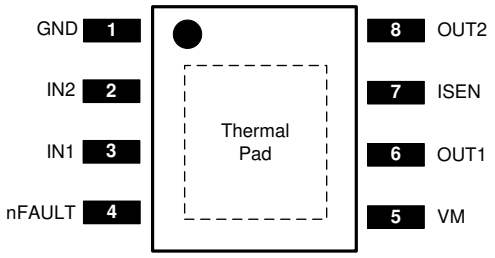

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Intended operation	D
IN2	2	OUTx driver control will be lost	B
IN1	3	OUTx driver control will be lost	B
nFAULT	4	Device will always signal fault	B
VM	5	Device will not power up	B
OUT1	6	OUTx HiZ, with device signaling fault	B
ISEN	7	Current regulation capability will be lost	B
OUT2	8	OUTx HiZ, with device signaling fault	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device will not power up	B
IN2	2	OUTx driver control will be lost	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN1	3	OUTx driver control will be lost	B
nFAULT	4	Fault signaling will be lost	B
VM	5	Device will not power up	B
OUT1	6	OUT1 driver control will be lost	B
ISEN	7	OUT1 and OUT2 driver control will be lost	B
OUT2	8	OUT2 driver control will be lost	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	IN2	OUTx driver control will be lost	B
IN2	2	IN1	OUTx driver control will be lost	B
IN1	3	nFAULT	OUTx driver control will be lost, fault signaling will be lost	B
nFAULT	4	VM	Low voltage pin max voltage violated	A
VM	5	OUT1	OUTx HiZ, with device signaling fault	B
OUT1	6	ISEN	Low voltage pin max voltage violated	A
ISEN	7	OUT2	Low voltage pin max voltage violated	A
OUT2	8	GND	OUTx HiZ, with device signaling fault	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device will not power up	B
IN2	2	Low voltage pin max voltage violated	A
IN1	3	Low voltage pin max voltage violated	A
nFAULT	4	Low voltage pin max voltage violated	A
VM	5	Intended operation	D
OUT1	6	OUTx HiZ, with device signaling fault	B
ISEN	7	Low voltage pin max voltage violated	A
OUT2	8	OUTx HiZ, with device signaling fault	B

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