*Functional Safety Information*

# *LM5157-Q1 and LM51571-Q1 Functional Safety FIT Rate, FMD, and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for LM5157-Q1 and LM51571-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device

Figure 1-1 shows the device functional block diagram for reference.

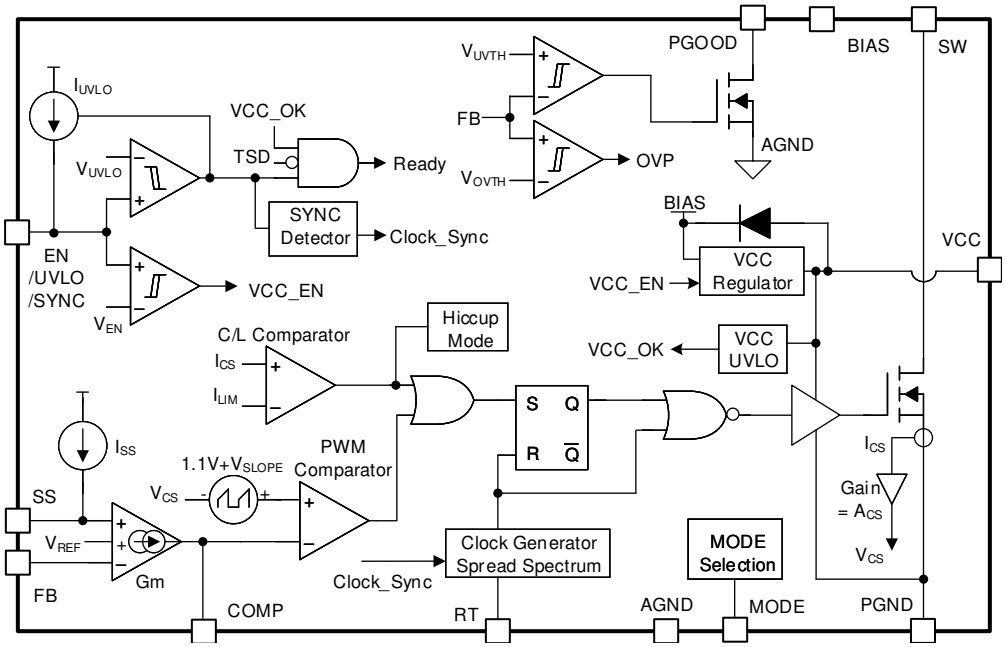


**Figure 1-1. Functional Block Diagram**

LM5157-Q1 and LM51571-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM5157-Q1 and LM51571-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 15 |
| Die FIT Rate | 8 |
| Package FIT Rate | 7 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 850 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS/BICMOS ASIC<br>Analog and Mixed ≤50 V supply | 25 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5157-Q1 and LM51571-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| SW no output | 40% |
| SW output not in specification – voltage or timing | 50% |
| SW power low-side FET stuck on | 5% |
| Power Good – False Trip or Failure to Trip | 5% |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM5157-Q1 and LM51571-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Figure 4-1 shows the LM5157-Q1 and LM51571-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM5157-Q1 and LM51571-Q1 data sheet.

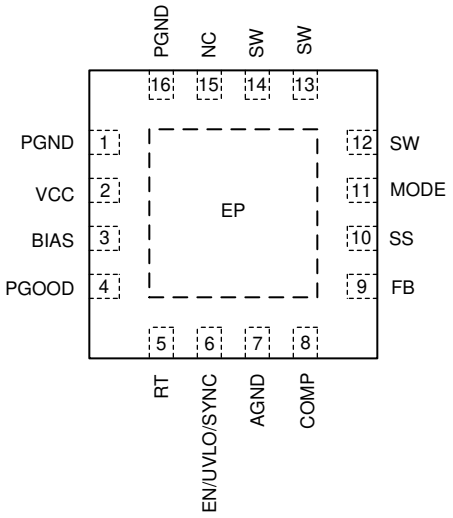


**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the LM5157-Q1 and LM51571-Q1 data sheet.
- Configuration as boost converter as shown in the *Application and Implementation* found in the LM5157-Q1 and LM51571-Q1 data sheet.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| PGND | 1, 16 | No effect. Normal operation | D |
| VCC | 2 | VCC regulator short circuit. The device can shut down due to thermal shutdown. | B |
| BIAS | 3 | The device is unpowered. The device is not functional. | B |
| PGOOD | 4 | Correct output voltage. Loss of power good functionality | B |
| RT | 5 | Switching frequency increased to > 2.2 MHz. The device can be unstable. | B |

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| EN/UVLO/SYNC | 6 | EN stuck low. The device is disabled and in shutdown mode. | B |
| AGND | 7 | No effect. Normal operation | D |
| COMP | 8 | Device out of regulation. The device is not switching. | B |
| FB | 9 | Output voltage rises and can exceed the absolute maximum rating of the SW pin voltage. Potential damage to pin | A |
| SS | 10 | During soft start, the SS pin is stuck low. The device does not start up. The device stops switching during operation. | B |
| MODE | 11 | Hiccup mode protection is disabled and spread spectrum is disabled. | B |
| NC | 12, 15 | No effect. Normal operation | D |
| SW | 13, 14 | Potential damage to inductor and pin | A |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| PGND | 1, 16 | Possible device damage | A |
| VCC | 2 | High ripple on VCC pin that can trigger VCC UVLO | B |
| BIAS | 3 | The device is unpowered. The device is not functional. | B |
| PGOOD | 4 | Correct output voltage. Loss of power-good functionality | C |
| RT | 5 | Internal oscillator is instable or not functional. The device stops switching operation. | B |
| EN/UVLO/SYNC | 6 | State of EN/UVLO/SYNC undetermined. Device can be in shutdown or standby mode or enabled. | B |
| AGND | 7 | Possible device damage | A |
| COMP | 8 | The device can be unstable. | C |
| FB | 9 | Output voltage is out of regulation. | B |
| SS | 10 | During soft start, the SS pin pulled high. The device soft-start time is reduced to 0. High inrush current possible. No effect during operation | C |
| MODE | 11 | Hiccup mode protection is disabled and spread spectrum is enabled. No effect during operation | B |
| NC | 12, 15 | No effect. Normal operation | D |
| SW | 13, 14 | Output voltage is out of regulation. Output voltage is equal to the input voltage minus diode forward voltage drop. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| PGND | 1 | VCC | VCC regulator short circuit. Device can shut down due to thermal shutdown. | B |
| VCC | 2 | BIAS | Potential device damage if BIAS voltage is greater 5.8 V | A |
| BIAS | 3 | PGOOD | Potential device damage if BIAS voltage is greater 18 V | A |
| PGOOD | 4 | RT | Loss of power-good functionality. Switching frequency is wrong. | B |
| RT | 5 | EN/UVLO/SYNC | EN pin voltage at enable threshold. The device is either disabled and in shutdown mode or in standby mode. | B |
| EN/UVLO/SYNC | 6 | AGND | EN stuck low. The device is disabled and in shutdown mode. | B |
| AGND | 7 | COMP | The device is out of regulation. The device is not switching. | B |
| COMP | 8 | FB | COMP and FB pin voltage are clamped to 1 V. The device is not switching and out of regulation. | B |
| FB | 9 | SS | COMP pin voltage clamped to 1 V. The device is not switching and out of regulation. | B |
| SS | 10 | MODE | MODE pin pulled low during read out. Hiccup mode protection is disabled and spread spectrum is disabled. | B |
| MODE | 11 | NC | No effect. Normal operation | D |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| NC | 12 | SW | No effect. Normal operation | D |
| SW | 13 | SW | No effect. Normal operation | D |
| SW | 14 | NC | No effect. Normal operation | D |
| NC | 15 | PGND | No effect. Normal operation | D |
| PGND | 16 | PGND | No effect. Normal operation | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to BIAS supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| PGND | 1, 16 | The device is unpowerered and not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage can be plausible. | A |
| VCC | 2 | Potential device damage if BIAS voltage is greater 5.8 V | A |
| BIAS | 3 | No effect. Normal operation | D |
| PGOOD | 4 | Potential device damage if BIAS voltage is greater 18 V | A |
| RT | 5 | Potential device damage if BIAS voltage is greater 3.8 V | A |
| EN/UVLO/SYNC | 6 | No effect. Normal operation | D |
| AGND | 7 | The device is unpowered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage can be plausible. | A |
| COMP | 8 | Potential device damage | A |
| FB | 9 | Potential device damage if BIAS voltage is greater 4.0 V | A |
| SS | 10 | Potential device damage if BIAS voltage is greater 3.8 V | A |
| MODE | 11 | Potential device damage if BIAS voltage is greater 3.8 V | A |
| NC | 12, 15 | No effect. Normal operation | D |
| SW | 13, 14 | Inductor out of regulation loop. Device is not functional. | B |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (December 2020) to Revision A (February 2022) | Page |
|---|---|
| • Added pin-FMA | 5 |

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265