Functional Safety Information

TPS1H000-Q1
Functional Safety FIT Rate, FMD, and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS1H000-Q1 (HVSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

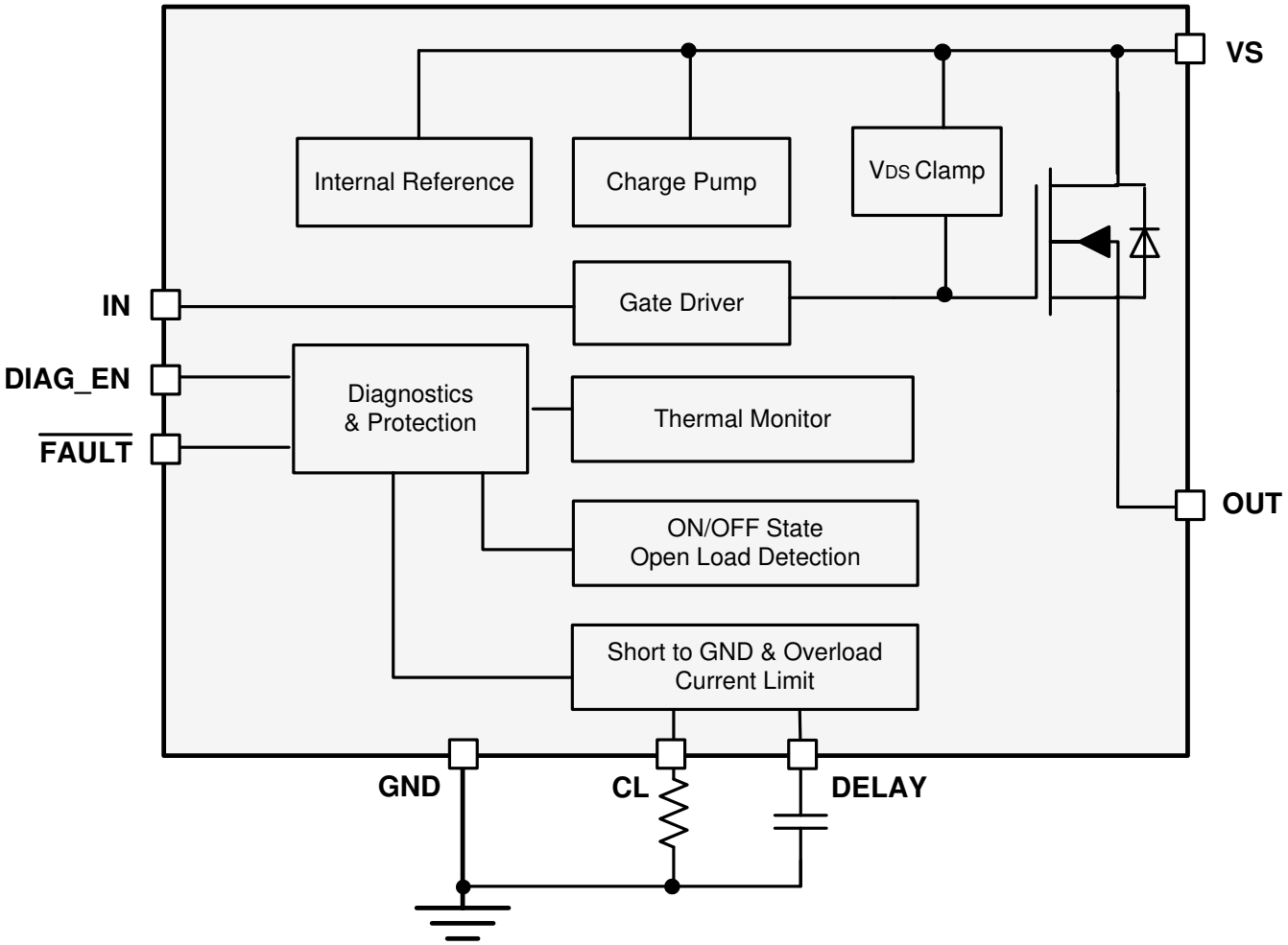

Figure 1-1. Functional Block Diagram

TPS1H000-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS1H000-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	6
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS1H000-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT stuck open (HiZ)	20%
VOUT stuck on (VS)	10%
VOUT functional, not in specification voltage or timing	45%
Diagnostics not in specification	10%
Protection function fails to trip	10%
Pin to Pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS1H000-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS1H000-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS1H000-Q1 data sheet.

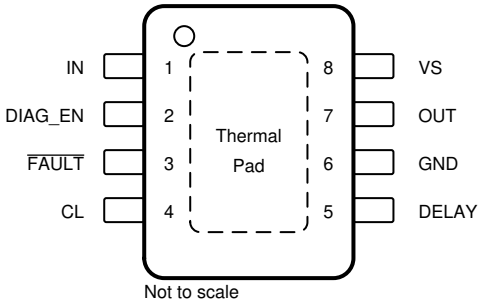

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follow data sheet recommendation for operating conditions, external component selection and PCB layout.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	Normal operation with output off (FET turned off).	B
DIAG_EN	2	Normal operation with diagnostics function disabled.	B
FAULT	3	Open drain fault diagnostics cannot be reported.	B
CL	4	Current limit defaults to internal limit.	C
DELAY	5	Normal operation with device in holding mode as defined in the data sheet.	B
GND	6	Resistor/diode network will be bypassed if present.	B
OUT	7	Short to GND protection kicks in to protect the device.	B
VS	8	Device will have no input supply and will not function.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	Output will be shut off because the pin is pulled down internally.	B
DIAG_EN	2	Diagnostics will be disabled as the pin is pulled down internally.	B
FAULT	3	Open drain fault diagnostics cannot be reported.	B
CL	4	Device will not be able to provide output current.	B
DELAY	5	Normal operation with device in auto-retry mode because the pin is pulled up internally.	B
GND	6	Resistor/diode network will be bypassed if present.	B
OUT	7	Loss of ground detection engages and device shuts off.	B
VS	8	Device will have no input supply and will not function.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	2 (DIAG_EN)	IN will affect DIAG_EN and vice versa. Diagnostics and the channel will be enabled if pin voltage > VIH; diagnostics and channel will be disabled if pin voltage < VIL.	B
DIAG_EN	2	3 (FAULT)	Undefined device behavior depends on pin voltage. Diagnostics will be enabled if pin voltage > VIH; diagnostics will be disabled if pin voltage < VIL. Open drain fault reporting could not be correct.	B
FAULT	3	4 (CL)	Open drain fault reporting could not be correct. Current limit would not be anticipated value.	B
DELAY	5	6 (GND)	Device would be in the holding mode as defined in the data sheet.	B
GND	6	7 (OUT)	Short to ground protection would kick in. Device would be protected.	B
OUT	7	8 (VS)	Short to battery detection would be triggered if configured. Device cannot turn off output.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	Normal operation with output turned on.	B
DIAG_EN	2	Normal operation with diagnostics turned on.	B
FAULT	3	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
CL	4	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
DELAY	5	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
GND	6	Supply power will be bypassed and device will not turn on.	B
OUT	7	Output will be pulled to supply voltage. Short-to-battery detection will be triggered if configured.	B
VS	8	Device functions as intended.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (July 2021) **Page**

- Added Table 2-2 3

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