Functional Safety Information

DP83TG720x-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the DP83TG720S-Q1 and DP83TG720R-Q1 to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

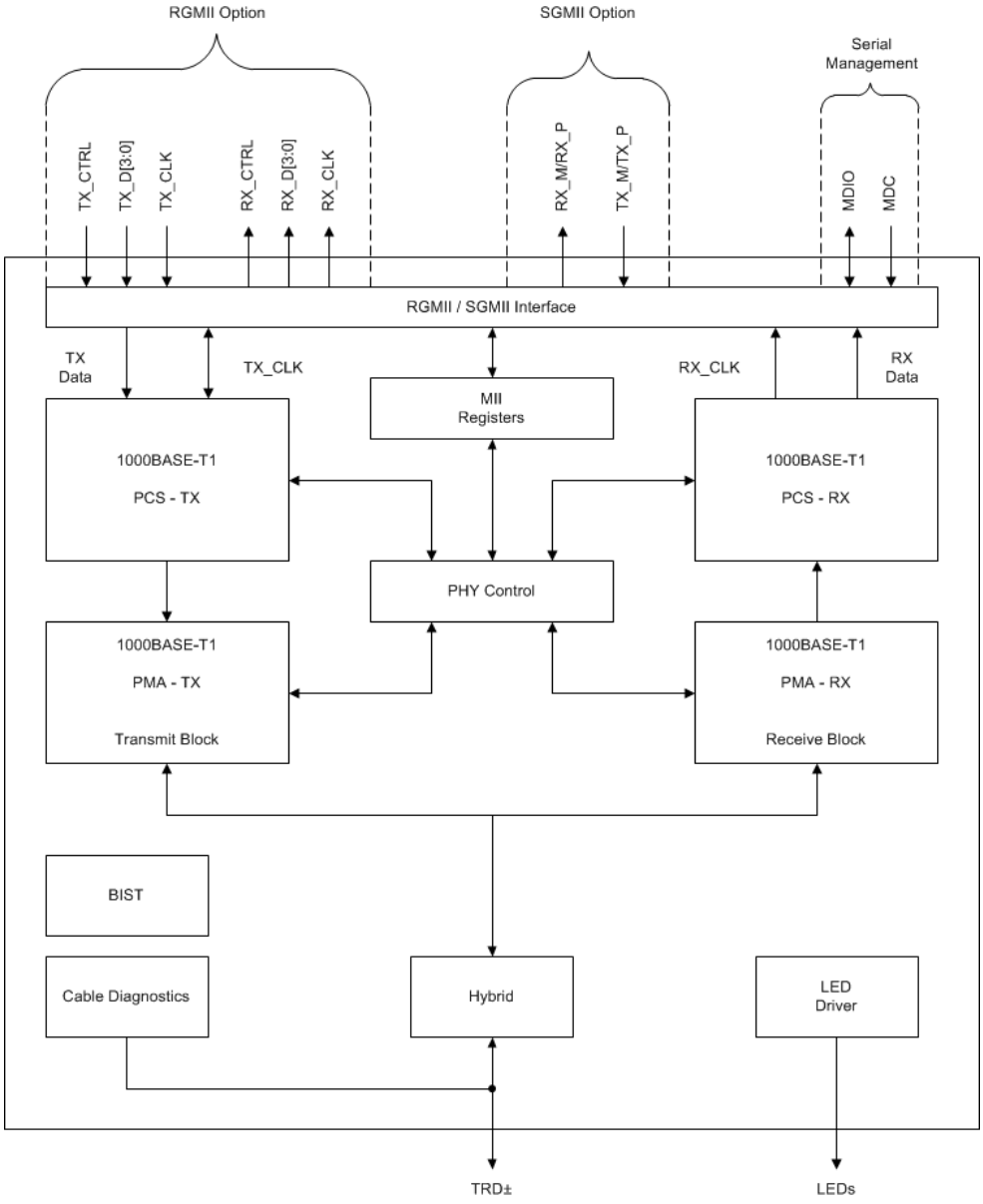

Figure 1-1. Functional Block Diagram

The DP83TG720S-Q1 and DP83TG720R-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the DP83TG720S-Q1 and DP83TG720R-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	26
Die FIT rate	3
Package FIT rate	23

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 590mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the DP83TG720S-Q1 and DP83TG720R-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Fault in MDI transmitter causes IEEE specification compliance issues	6
Fault in MDI transmitter causes high RF emissions	3
Fault in MDI receiver causes poor link quality and poor link loss	5
Fault in internal power circuits causes poor link quality and higher power consumption	7
Fault in internal clock circuits cause IEEE compliance issues and poor link quality	5
Fault in GPIO causes higher RF emissions	5
Fault in GPIO causes RGMII, JEDEC, and data sheet specification violation	4
Fault in ESD on MDI makes IEC ESD performance lower than 8KV	3
Fault in ESD on GPIOs makes CDM performance lower than 2KV	2
Digital core has stuck or transient faults that cause link-up or PCS faults	60

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the DP83TG720x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDDIO (see Table 4-5)
- Pin short-circuited to VDD1P0 (see Table 4-6)
- Pin short-circuited to VDDA (see Table 4-7)
- Pin short-circuited to VSLEEP (see Table 4-8)

Table 4-2 through Table 4-8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the DP83TG720S-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the DP83TG720S-Q1 data sheet.

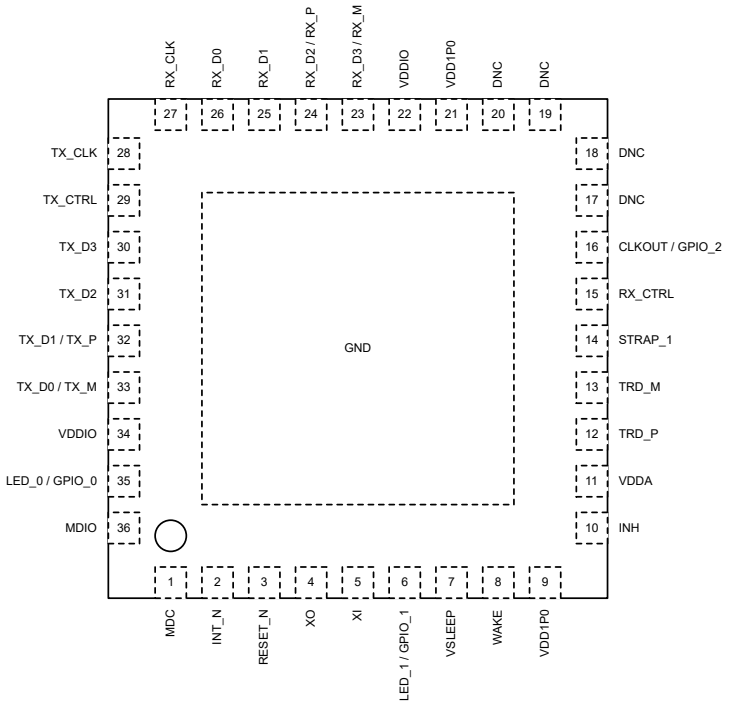

Figure 4-1. DP83TG720S-Q1 Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MDC	1	No SMI communication is available.	B
INT_N	2	No valid interrupt status.	B
RESET_N	3	Device in reset state.	B
XO	4	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	A
XI	5	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	B
LED_1/GPIO_1	6	LED_1/GPIO_1 is not operational.	A
VSLEEP	7	Device is disabled. Core supply is short.	B
WAKE	8	Device is unable to locally wake from sleep state.	B
VDD1P0	9	Device is disabled. Core supply is short.	B
INH	10	Inhibit is not operational.	B
VDDA	11	Device is disabled. Core supply is short.	B
TRD_P	12	Link and data transfer cannot occur. Device can be damaged.	A
TRD_M	13	Link and data transfer cannot occur. Device can be damaged.	A
STRAP_1	14	PHY address can strap incorrectly.	B
RX_CTRL	15	PHY address can strap incorrectly. Valid data cannot be sent to MAC. Device can be damaged.	A
CLKOUT/GPIO_2	16	CLKOUT/GPIO_2 is not operational. Device can be damaged.	A
DNC	17	Device can be damaged.	A
DNC	18	No issue.	D
DNC	19	No issue.	D
DNC	20	No issue.	D
VDD1P0	21	Device is disabled. Core supply is short.	B
VDDIO	22	Device is disabled. Core supply is short	B
RX_D3/RX_M	23	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D2/RX_P	24	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D1	25	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D0	26	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_CLK	27	Valid data cannot be sent to MAC. Device can be damaged.	A
TX_CLK	28	Valid data cannot be received.	B
TX_CTRL	29	Valid data cannot be received.	B
TX_D3	30	Valid data cannot be received.	B
TX_D2	31	Valid data cannot be received.	B
TX_D1/TX_P	32	Valid data cannot be received.	B
TX_D0/TX_M	33	Valid data cannot be received.	B
VDDIO	34	Device is disabled. Core supply is short.	B
LED_0/GPIO_0	35	LED_0/GPIO_0 is not operational. Master and slave strap is sampled as slave. Device can be damaged.	A
MDIO	36	No SMI communication is available. Device can be damaged.	A
DAP	GND	Appropriate connection.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MDC	1	No SMI communication is available.	B
INT_N	2	Interrupt is not available.	B
RESET_N	3	Normal operation.	D
XO	4	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	B
XI	5	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown	B
LED_1/GPIO_1	6	LED_1/GPIO_1 is not operational. PHY enters autonomous mode.	B
VSLEEP	7	Device is disabled. VSLEEP supply is open.	B
WAKE	8	Wake functionality is lost.	B
VDD1P0	9	Device is disabled. VDD1P0 supply is open.	B
INH	10	Inhibit is not operational.	B
VDDA	11	Device is disabled. Core supply is open.	B
TRD_P	12	Link and data transfer cannot occur.	B
TRD_M	13	Link and data transfer cannot occur.	B
STRAP_1	14	PHY address can strap incorrectly.	B
RX_CTRL	15	PHY address can strap incorrectly. Valid data cannot be sent to MAC.	B
CLKOUT/GPIO_2	16	CLKOUT/GPIO_2 is not operational.	B
DNC	17	No issue.	D
DNC	18	No issue.	D
DNC	19	No issue.	D
DNC	20	No issue.	D
VDD1P0	21	Device is disabled. VDD1P0 supply is open.	B
VDDIO	22	Device is disabled. VDDIO supply is open.	B
RX_D3/RX_M	23	Valid data cannot be sent to MAC.	B
RX_D2/RX_P	24	Valid data cannot be sent to MAC.	B
RX_D1	25	Valid data cannot be sent to MAC.	B
RX_D0	26	Valid data cannot be sent to MAC.	B
RX_CLK	27	Valid data cannot be sent to MAC.	B
TX_CLK	28	Valid data cannot be received.	B
TX_CTRL	29	Valid data cannot be received.	B
TX_D3	30	Valid data cannot be received.	B
TX_D2	31	Valid data cannot be received.	B
TX_D1/TX_P	32	Valid data cannot be received.	B
TX_D0/TX_M	33	Valid data cannot be received.	B
VDDIO	34	Device is disabled. VDDIO supply is open.	B
LED_0/GPIO_0	35	LED_0/GPIO_0 is not operational. Master and slave strap is sampled as slave.	B
MDIO	36	No SMI communication is available.	B
DAP	GND	Ground is open.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
MDC	1	INT_N	No SMI communication is available. No valid interrupt status.	B
INT_N	2	RESET_N	When the device intends to give an interrupt, the device enters reset, and when the host resets the PHY, the host is ISR triggered.	B
RESET_N	3	XO	Device keeps resetting.	B
XO	4	XI	Device is in an unknown state.	B
XI	5	LED_1/GPIO_1	Device is in an unknown state.	B
LED_1/GPIO_1	6	VSLEEP	Device can be damaged.	A
VSLEEP	7	WAKE	Wake functionality is lost.	B
WAKE	8	VDD1P0	Wake functionality is lost.	B
VDD1P0	9	INH	Inhibit is not operational.	B
INH	10	VDDA	Inhibit is not operational.	B
VDDA	11	TRD_P	Link and data transfer cannot occur. Device can be damaged.	A
TRD_P	12	TRD_M	Link and data transfer cannot occur.	B
TRD_M	13	STRP_1/GPIO_6	Link and data transfer cannot occur.	B
STRP_1/ GPIO_6	14	RX_CTRL	Valid data cannot be sent to MAC.	B
RX_CTRL	15	CLKOUT/GPIO_2	Valid data cannot be sent to MAC. CLKOUT/GPIO_2 is not functional.	B
CLKOUT/ GPIO_2	16	DNC	Device can be damaged.	A
DNC	17	DNC	Device can be disabled.	B
DNC	18	DNC	No issue.	D
DNC	19	DNC	No issue.	D
DNC	20	VDD1P0	Device can be damaged.	A
VDD1P0	21	VDDIO	Device can be damaged.	A
VDDIO	22	RX_D3/RX_M	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D3/RX_M	23	RX_D2/RX_P	MAC interface selection can be corrupt. Valid data cannot be sent to MAC.	B
RX_D2/RX_P	24	RX_D1	MAC interface selection can be corrupt. Valid data cannot be sent to MAC.	B
RX_D1	25	RX_D0	MAC interface selection can be corrupt. Valid data cannot be sent to MAC.	B
RX_D0	26	RX_CLK	MAC interface selection can be corrupt. Valid data cannot be sent to MAC.	B
RX_CLK	27	TX_CLK	Valid data cannot be exchanged with MAC.	B
TX_CLK	28	TX_CTRL	Valid data cannot be received.	B
TX_CTRL	29	TX_D3	Valid data cannot be received.	B
TX_D3	30	TX_D2	Valid data cannot be received.	B
TX_D2	31	TX_D1/TX_P	Valid data cannot be received.	B
TX_D1/TX_P	32	TX_D0/TX_M	Valid data cannot be received.	B
TX_D0/TX_M	33	VDDIO	Valid data cannot be received.	B
VDDIO	34	LED_0/GPIO_0	Valid data cannot be received.	B
LED_0/GPIO_0	35	MDIO	No SMI communication is available.	B
MDIO	36	MDC	No SMI communication is available.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDDIO

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MDC	1	No SMI communication is available.	B
INT_N	2	No valid interrupt status.	B
RESET_N	3	The device can never be reset.	B
XO	4	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	A
XI	5	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	B
LED_1/GPIO_1	6	LED_1/GPIO_1 is not operational. Device enters standby mode. Need register write to start link-up. Device can be damaged.	A
VSLEEP	7	PHY not powering up is possible if VDDIO < 3.3V.	B
WAKE	8	The device not entering sleep state is possible.	B
VDD1P0	9	Device can be damaged.	A
INH	10	Inhibit is not operational.	B
VDDA	11	The device not powering up is possible.	B
TRD_P	12	Link and data transfer cannot occur. Device can be damaged.	A
TRD_M	13	Link and data transfer cannot occur. Device can be damaged.	A
STRAP_1	14	PHY address can strap incorrectly.	B
RX_CTRL	15	PHY address can strap incorrectly. Valid data cannot be sent to MAC.	B
CLKOUT/GPIO_2	16	CLKOUT/GPIO_2 is not operational.	B
DNC	17	Device can be damaged.	A
DNC	18	Device can be damaged.	A
DNC	19	Device can be damaged.	A
DNC	20	Device can be damaged.	A
VDD1P0	21	Device can be damaged.	A
VDDIO	22	No issue.	D
RX_D3/RX_M	23	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D2/RX_P	24	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D1	25	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D0	26	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_CLK	27	Valid data cannot be sent to MAC. Device can be damaged.	A
TX_CLK	28	Valid data cannot be received.	B
TX_CTRL	29	Valid data cannot be received.	B
TX_D3	30	Valid data cannot be received.	B
TX_D2	31	Valid data cannot be received	B
TX_D1/TX_P	32	Valid data cannot be received.	B
TX_D0/TX_M	33	Valid data cannot be received.	B
VDDIO	34	No issue.	D
LED_0/GPIO_0	35	LED_0/GPIO_0 is not operational. Master and slave strap is sampled as master. Device can be damaged.	A
MDIO	36	No SMI communication is available. Device can be damaged.	A
DAP	GND	Device can be damaged.	A

Table 4-6. Pin FMA for Device Pins Short-Circuited to VDD1P0

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MDC	1	No SMI communication. Device can be damaged.	A
INT_N	2	Device can be damaged	A
RESET_N	3	The device entering reset state is possible.	B
XO	4	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	B
XI	5	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	B
LED_1/GPIO_1	6	LED_1/GPIO_1 is not operational, Device can enter standby mode. Need register write to start link-up.	B
VSLEEP	7	Device does not power-up.	B
WAKE	8	Device does not go into sleep state.	B
VDD1P0	9	Appropriate connection.	D
INH	10	Inhibit is not operational.	B
VDDA	11	Device can be damaged.	A
TRD_P	12	Link and data transfer cannot occur. Device can be damaged.	A
TRD_M	13	Link and data transfer cannot occur. Device can be damaged.	A
STRAP_1	14	PHY address can strap incorrectly.	B
RX_CTRL	15	PHY address can strap incorrectly. Valid data cannot be sent to MAC.	B
CLKOUT/GPIO_2	16	CLKOUT/GPIO_2 is not operational.	B
DNC	17	Device can be damaged.	A
DNC	18	Device can be damaged.	A
DNC	19	Device can be damaged.	A
DNC	20	Device can be damaged.	A
VDD1P0	21	Appropriate connection.	D
VDDIO	22	The device not powering up is possible.	B
RX_D3/RX_M	23	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D2/RX_P	24	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D1	25	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_D0	26	Valid data cannot be sent to MAC. Device can be damaged.	A
RX_CLK	27	Valid data cannot be sent to MAC. Device can be damaged.	A
TX_CLK	28	Valid data cannot be received.	B
TX_CTRL	29	Valid data cannot be received.	B
TX_D3	30	Valid data cannot be received.	B
TX_D2	31	Valid data cannot be received.	B
TX_D1/TX_P	32	Valid data cannot be received.	B
TX_D0/TX_M	33	Valid data cannot be received.	B
VDDIO	34	The device not powering up is possible.	B
LED_0/GPIO_0	35	LED_0/GPIO_0 is not operational. Master and slave strap can be sampled incorrectly. Device can be damaged.	A
MDIO	36	No SMI communication is available. Device can be damaged.	A
DAP	GND	Device can be damaged.	A

Table 4-7. Pin FMA for Device Pins Short-Circuited to VDDA

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MDC	1	No SMI communication. Device can be damaged.	A
INT_N	2	Device can be damaged.	A
RESET_N	3	Device can be damaged.	A
XO	4	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	A
XI	5	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	B
LED_1/GPIO_1	6	Device can be damaged.	A
VSLEEP	7	Device is functional.	D
WAKE	8	Device does not go into sleep state.	B
VDD1P0	9	Device can be damaged.	A
INH	10	Inhibit is not operational.	B
VDDA	11	Appropriate connection.	D
TRD_P	12	Link and data transfer cannot occur. Device can be damaged.	A
TRD_M	13	Link and data transfer cannot occur. Device can be damaged.	A
STRAP_1	14	Device can be damaged.	A
RX_CTRL	15	Device can be damaged.	A
CLKOUT/GPIO_2	16	Device can be damaged.	A
DNC	17	Device can be damaged.	A
DNC	18	Device can be damaged.	A
DNC	19	Device can be damaged.	A
DNC	20	Device can be damaged.	A
VDD1P0	21	Device can be damaged.	A
VDDIO	22	Device can power up in the wrong state.	B
RX_D3/RX_M	23	Device can be damaged.	A
RX_D2/RX_P	24	Device can be damaged.	A
RX_D1	25	Device can be damaged.	A
RX_D0	26	Device can be damaged.	A
RX_CLK	27	Device can be damaged.	A
TX_CLK	28	Device can be damaged.	A
TX_CTRL	29	Device can be damaged.	A
TX_D3	30	Device can be damaged.	A
TX_D2	31	Device can be damaged.	A
TX_D1/TX_P	32	Device can be damaged.	A
TX_D0/TX_M	33	Device can be damaged.	A
VDDIO	34	Device can power up in the wrong state.	B
LED_0/GPIO_0	35	Device can be damaged.	A
MDIO	36	No SMI communication is available. Device can be damaged.	A
DAP	GND	Device can be damaged.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to VSLEEP

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MDC	1	No SMI communication. Device can be damaged.	A
INT_N	2	Device can be damaged.	A
RESET_N	3	Device can be damaged.	A
XO	4	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	A
XI	5	Crystal resonator clock does not start-up. Device PLL is not operational. PHY state is unknown.	B
LED_1/GPIO_1	6	Device can be damaged.	A
VSLEEP	7	Appropriate connection.	D
WAKE	8	Device does not go into sleep state.	B
VDD1P0	9	Device can be damaged.	A
INH	10	Inhibit is not operational.	B
VDDA	11	Device is functional.	D
TRD_P	12	Link and data transfer cannot occur. Device can be damaged.	A
TRD_M	13	Link and data transfer cannot occur. Device can be damaged.	A
STRAP_1	14	Device can be damaged.	A
RX_CTRL	15	Device can be damaged.	A
CLKOUT/GPIO_2	16	Device can be damaged.	A
DNC	17	Device can be damaged.	A
DNC	18	Device can be damaged.	A
DNC	19	Device can be damaged.	A
DNC	20	Device can be damaged.	A
VDD1P0	21	Device can be damaged.	A
VDDIO	22	Device can power up in the wrong state.	B
RX_D3/RX_M	23	Device can be damaged.	A
RX_D2/RX_P	24	Device can be damaged.	A
RX_D1	25	Device can be damaged.	A
RX_D0	26	Device can be damaged.	A
RX_CLK	27	Device can be damaged.	A
TX_CLK	28	Device can be damaged.	A
TX_CTRL	29	Device can be damaged.	A
TX_D3	30	Device can be damaged.	A
TX_D2	31	Device can be damaged.	A
TX_D1/TX_P	32	Device can be damaged.	A
TX_D0/TX_M	33	Device can be damaged.	A
VDDIO	34	Device can power up in the wrong state.	B
LED_0/GPIO_0	35	Device can be damaged.	A
MDIO	36	No SMI communication is available. Device can be damaged.	A
DAP	GND	Device can be damaged.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265