Functional Safety Information

TPS62816-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS62816-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

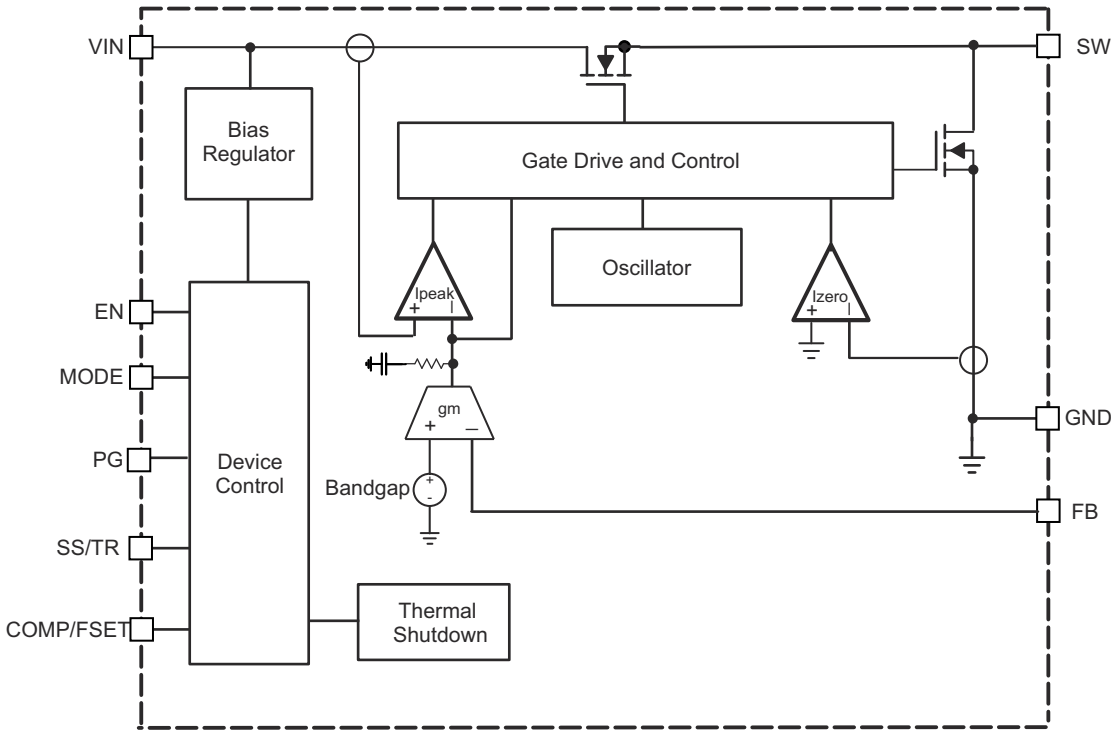

Figure 1-1. Functional Block Diagram

TPS62816-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS62816-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	6
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 597 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS62816-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35%
SW output not in specification – voltage or timing	45%
SW power HS or LS FET stuck on	10%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS62816-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS62816-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS62816-Q1 datasheet.

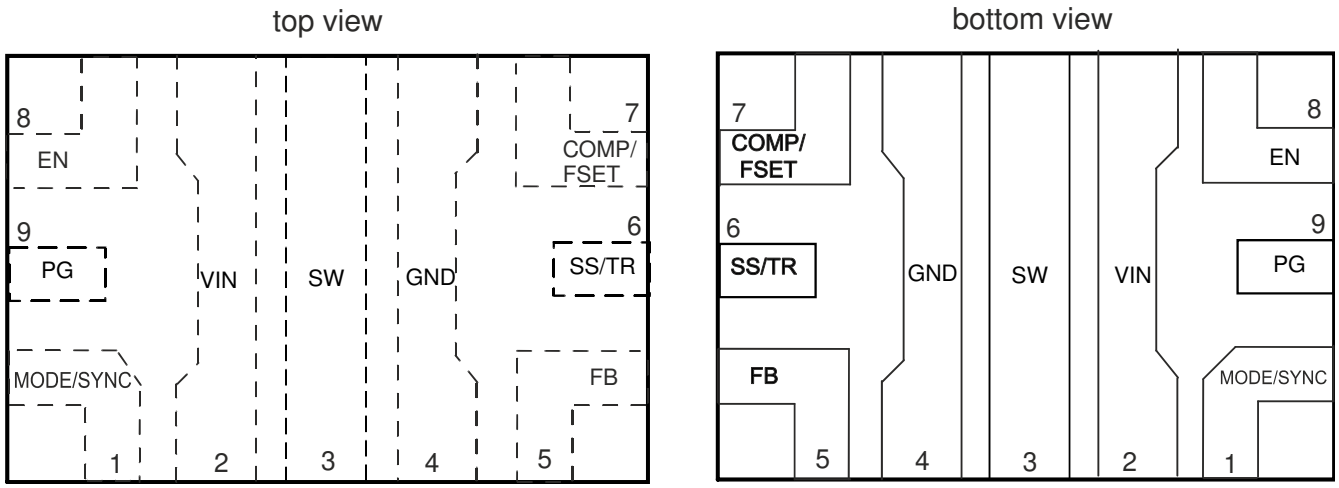

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption the device is running in the typical application, please refer to the 'Simplified Schematics' on the 1st page in the TPS62816-Q1 datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	Normal operation	D
VIN	2	Device does not power up, no output voltage	B
SW	3	Potential device damage	A
GND	4	Normal operation	D
FB	5	100% duty cycle mode, output voltage follows the input voltage	B
SS/TR	6	Device does not start properly, no output voltage	B
COMP/FSET	7	Normal operation	D
EN	8	Device is disabled, no output voltage	B
PG	9	Normal operation, no power good indication	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	Device either operates in forced PWM or power save mode enabled. Output voltage is regulated to its nominal value.	B
VIN	2	Device does not power up, no output voltage	B
SW	3	No output voltage	B
GND	4	Device does not power up, no output voltage	B
FB	5	100% or 0% duty cycle operation, no regulated output voltage. Output voltage either follows the input voltage or no output voltage	B
SS/TR	6	Normal operation	D
COMP/FSET	7	Normal operation	D
EN	8	Device is either enabled or disabled. If enabled, output voltage is regulated to its nominal value. If disabled no output voltage	B
PG	9	Normal operation	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	2	Normal operation	D
VIN	2	3	Potential device damage	A
SW	3	4	Potential device damage	A
GND	4	5	100% duty cycle mode, output voltage follows the input voltage	B
FB	5	6	0% duty cycle mode, no output voltage	B
SS/TR	6	7	Normal operation	D
COMP/FSET	7	4	Normal operation	D
EN	8	2	Normal operation	D
EN	8	9	Device does not power up, no output voltage	B
PG	9	1	Device operates in forced PWM once PG is high impedance. Output voltage is regulated to its nominal value.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	Normal operation	D
VIN	2	Normal operation	D
SW	3	Potential device damage	A
GND	4	Device does not power up, no output voltage	B
FB	5	Potential device damage	A
SS/TR	6	Normal operation	D
COMP/FSET	7	Normal operation	D
EN	8	Normal operation	D
PG	9	Potential device damage	A

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