Application Note

TCA6408A-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TCA6408A-Q1 (TSSOP PW package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

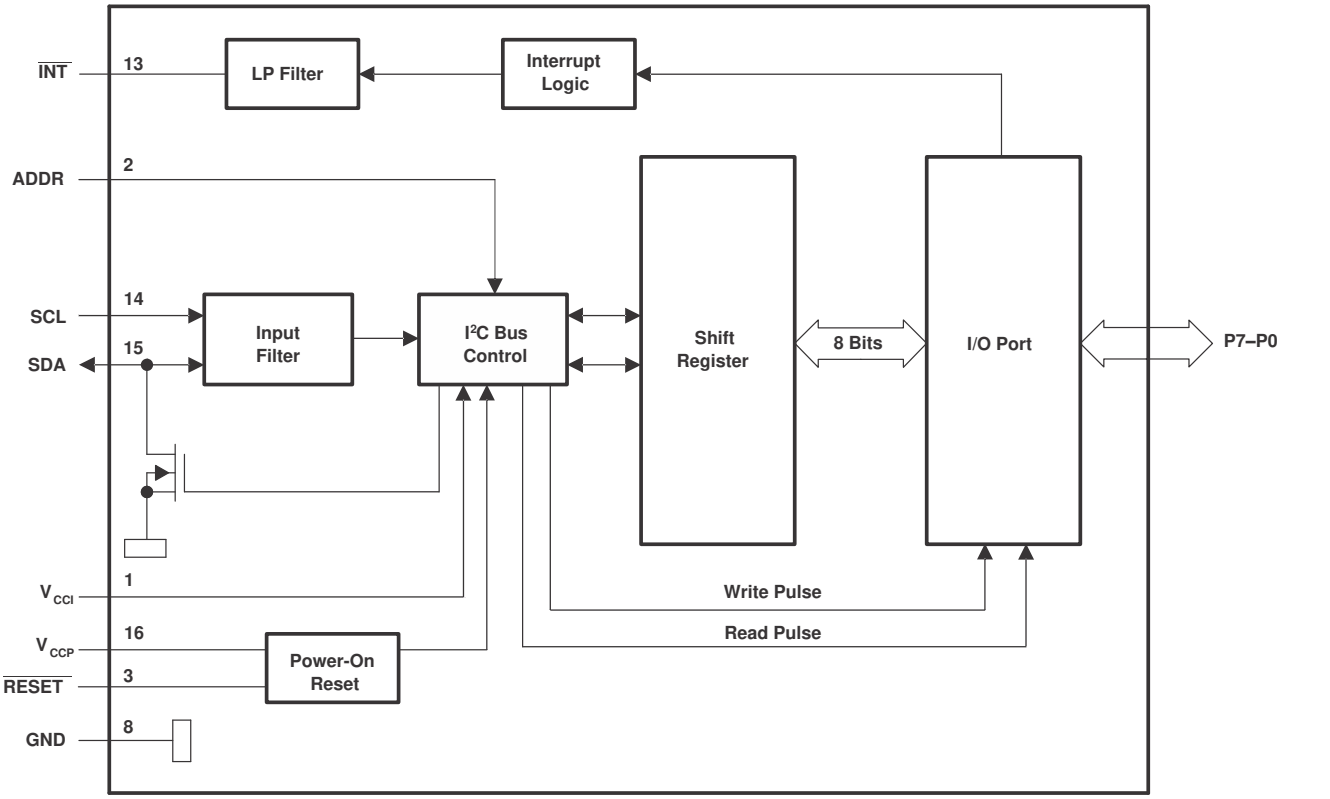

Figure 1-1. Functional Block Diagram

TCA6408A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCA6408A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	2
Package FIT Rate	9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 35 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCA6408A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
I2C control / communication error	15%
I/O data bit error	10%
I/O configuration error	15%
INT false trip, fails to trip	20%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCA6408A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TCA6408A-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCA6408A-Q1 data sheet.

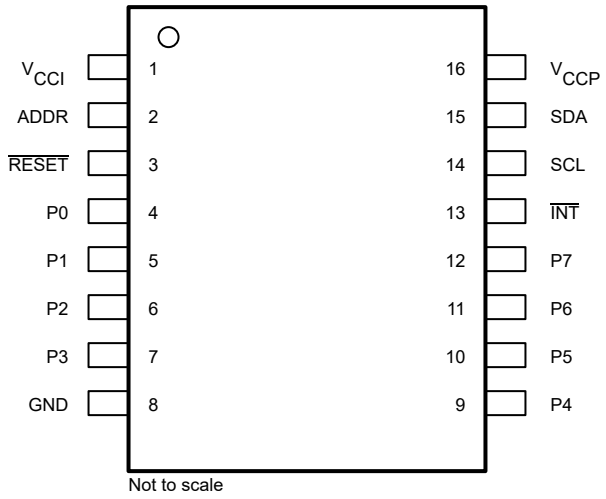

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- None

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{cci}	1	System short to GND. No damage to device expected.	B
ADDR	2	Potential functionality issue if ADDR is referenced to Vcc through a pull up resistor. On a system level, if ADDR is tied to Vcc through a resistor, then additional leakage current will occur through the resistor. On a system level, the I2C address of the device would change and the controller would not be able to communicate with the device. There would also be potential for signal integrity as there may be an address conflict on the bus. If ADDR is tied to GND via pull down resistor, then functionality is okay if ADDR were shorted to GND.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
#RESET	3	Functionality issue as the device would be held in the RESET state. On a system level, the controller would not be able to communicate with the device. The device would NACK its own address.	B
P0	4	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin never changes states and would not assert the INT function.	A
P1	5	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin never changes states and would not assert the INT function.	A
P2	6	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin never changes states and would not assert the INT function.	A
P3	7	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin never changes states and would not assert the INT function.	A
GND	8	No expected issue.	D
P4	9	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin never changes states and would not assert the INT function.	A
P5	10	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin never changes states and would not assert the INT function.	A
P6	11	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin never changes states and would not assert the INT function.	A
P7	12	Worst case situation: Pin is configured to be an output HIGH. A short to GND would cause high current draw from the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OH} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to GND, the pin will never change states and would not assert the INT function.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
#INT	13	Functionality lost as #INT is always be asserted. If controller is monitoring the #INT pin, the controller would always see #INT asserted (which may be false). Device damage is not expected though leakage current would be seen at a system level due to a path from Vcc to GND through the pull up resistor tied to #INT.	B
SCL	14	Functionality lost as SCL is stuck as a logic low. On a system level, this would lock the I2C bus. I2C communication would no longer work.	B
SDA	15	Functionality lost as SDA remains a logic low. On a system level, this would lock the I2C bus. I2C communication would no longer work.	B
V_{ccp}	16	System short to GND. No damage to device expected. Potential chance for SDA to be locked low. Please check datasheet's power supply recommendation section.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{cci}	1	Functionality lost. Device will not respond to its address, thus is not able to be configured or communicated with.	B
ADDR	2	Functionality may be lost. Device address may float meaning the I2C address of the device float to an unexpected value and the controller would not be able to communicate with the device. There would also be potential for signal integrity as there may be an address conflict on the bus if it floated to the opposite logic level of the external resistor reference.	B
#RESET	3	Functionality may be lost. If #RESET floats low, the device would be held in the RESET state. In this state, the device would not ACK its address would set all registers back to the default state.	B
P0	4	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B
P1	5	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B
P2	6	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B
P3	7	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B
GND	8	Damage could occur since the GND is used to bias substrates of FETs, power at pins while GND is floating may result in current to unexpected paths in device.	A
P4	9	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P5	10	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B
P6	11	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B
P7	12	Functionality lost. When pin is configured as an INPUT, any input changes would not be registered. If the input floats, the INT could falsely assert. Any input reads could provide incorrect values. When the pin is configured as an OUTPUT, the output state would not change at the pin. On a system level, the bias voltage at the pin would just float.	B
#INT	13	Functionality lost. #INT never asserts. On a system level, if controller is using #INT to determine input changes, it is missed.	B
SCL	14	Functionality lost. Device state machine may not see SCL toggle. Device would NACK its own address and would not be configurable.	B
SDA	15	Functionality lost. Device state machine may not see SDA toggle. Device would NACK its own address and would not be configurable.	B
V_{ccp}	16	Functionality lost. Device does not respond to its address, thus is not able to be configured or communicated with.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V_{cci}	1	ADDR	Potential functionality issue if ADDR is referenced to GND through a pull-down resistor. On a system level, if ADDR is tied to GND through a resistor, then additional leakage current will occur through the resistor. On a system level, the I2C address of the device would change and the controller would not be able to communicate with the device. There would also be potential for signal integrity as there may be an address conflict on the bus. If ADDR is tied to VCC via pull up resistor, then functionality is okay if ADDR were shorted to Vcc.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
ADDR	2	#RESET	#RESET is typically tied to a resistor referencing Vcc. Potential functionality issue if ADDR is referenced to GND through a pull-down resistor. Both the ADDR and #RESET pins will form a voltage divider between the pull up and pull down resistors. There is a potential for the device to float between the reset state and normal operation state. Any noise which couples to this node would also toggle the reset state. On a system level, the device may intermittently reset or could remain in reset depending on the node's voltage. Another possibility is the device is not in reset but the device's configurable address could change from the intended logic 0 to a logic 1 due to the voltage divider. On a system level, this could result in the device NACK'ing to the expected address or cause signal integrity issues due to a potential in conflicting I2C addresses. If the latter case is true, writes to the device could unintentionally set the p-port to be outputs or inputs when they were not intended to be. If ADDR is tied to VCC via pull up resistor, then funtionality-wise, the device should operate correctly if ADDR were shorted to #RESET.	B
#RESET	3	P0	If P0 is an INPUT (by default) and referenced with an external pull-up resistor then no functionality issues are expected. If P0 is an INPUT (by default) and referenced with an external pull-down resistor then P0 and #RESET form a voltage divider, and the voltage at these pins settle somewhere mid rail if pull-up and pull-down resistors are equal in value. #RESET and P0 may be in an unknown state because they are not above/below V_{IH} /V_{IL} levels. Noise coupling onto these pins may toggle reset. Assume functionality is lost. If P0 is configured to be an OUTPUT HIGH, device would NOT be reset and functionality should be okay. Some additional leakage may be present. If P0 is configured to be an OUTPUT LOW, device would be reset and then all GPIOs would return to their default power up state of an input. Functionality would be lost if P0 is ever configured to be an output LOW.	B
P0	4	P1	If P0 and P1 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If I_{oH} exceeds 50mA then damage may occur but may not be instantaneous. Failures overtime may occur. If P0 and P1 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), damage is not expected but some leakage current may occur. If P0 and P1 are both INPUTs, damage is not expected. If P0 and P1 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P1	5	P2	If P1 and P2 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If I_{oH} exceeds 50mA then damage may occur but may not be instantaneous. Failures overtime may occur. If P1 and P2 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), damage is not expected but some leakage current may occur. If P1 and P2 are both INPUTs, damage is not expected. If P1 and P2 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
P2	6	P3	If P2 and P3 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If I_{oH} exceeds 50mA then damage may occur but may not be instantaneous. Failures overtime may occur. If P2 and P3 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), damage is not expected but some leakage current may occur. If P2 and P3 are both INPUTs, damage is not expected. If P2 and P3 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P3	7	GND	If P3 is set to an OUTPUT LOW, no functionality or damage is expected. If P3 is an INPUT, no damage is expect but functionality will be lost as P3 will likely not see a logic HIGH and set the INT. If P3 is an OUTPUT HIGH, damage is likely to occur as a large I_{oH} current will flow from the pin and likely exceed the V_{oH} limit.	A
P4	9	P5	If P4 and P5 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If I_{oH} exceeds 50mA then damage may occur but may not be instantaneous. Failures overtime may occur. If P4 and P5 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), damage is not expected but some leakage current may occur. If P4 and P5 are both INPUTs, damage is not expected. If P4 and P5 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P5	10	P6	If P5 and P6 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If I_{oH} exceeds 50mA then damage may occur but may not be instantaneous. Failures overtime may occur. If P5 and P6 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), damage is not expected but some leakage current may occur. If P5 and P6 are both INPUTs, damage is not expected. If P5 and P6 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A
P6	11	P7	If P6 and P7 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If I_{oH} exceeds 50 mA, then damage may occur but may not be instantaneous. Failures overtime may occur. If P6 and P7 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), damage is not expected but some leakage current may occur. If P6 and P7 are both INPUTs, damage is not expected. If P6 and P7 are configured such that the pair is an OUTPUT and an INPUT, then no damage is expected.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
P7	12	#INT	If P7 is an INPUT then P7 will mirror #INT status. If P7 is an OUTPUT LOW, the #INT will get stuck low. On a system level, the controller would not be able to deassert #INT by reading the input port. If sw polls INT, then the controller is stuck reading the device. If P7 is an OUTPUT HIGH, when #INT is asserted, contention will occur between the P7 and the #INT's NFET. If the I_{OL} exceeds 25 mA, damage may occur.	A
#INT	13	SCL	From a device standpoint, no functionality loss or damage expected from this. From a system level, this may cause problems to the controller if it is monitoring #INT. The worst case issue is if #INT is asserted, the I2C bus would get stuck low unless #INT deasserts which may not happen depending on how the input that changed is set up.	B
SCL	14	SDA	I2C communication is lost both to the device and to the system's I2C bus. Functionality will be lost but no damage expected.	B
SDA	15	V_{ccp}	Device is likely to be damaged during ACKs and read transaction due to large excessive current through pin. If IoL exceeds 6 mA at 85°C or less, device may be damaged. Damage may not be instantaneous, but may occur over time. V_{OL} from device may also be too large for the controller to accept as a valid low during ACKs.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{cci}	1	If supply voltage is the same voltage as V_{cci} then no issue is expected. If supply voltage is not the same voltage as V_{cci} and is within absolute maximum specification then no damage is expected to the device. On a system level, high current may occur due to a short between two voltage rails. If supply voltage is larger than the absolute maximum specification for the device, damage could occur.	A
ADDR	2	Potential funtionality issue if ADDR is referenced to GND through a pull-down resistor. On a system level, if ADDR is tied to GND through a resistor, then additional leakage current occurs through the resistor. On a system level, the I2C address of the device would change and the controller would not be able to communicate with the device. There would also be potential for signal integrity as there may be an address conflict on the bus. If ADDR is tied to VCC via pull up resistor, then functionality is okay if ADDR were shorted to Vcc.	B
#RESET	3	Device would maintain functionality though from a system level, the controller would not be able to drive the #RESET low to reset the device. Any attempts to do so could damage the controller due to high current from Vcc to GND from the low side driver of the controller.	D
P0	4	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin never changes states and would not assert the INT function.	A
P1	5	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin never changes states and would not assert the INT function.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
P2	6	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin never changes states and would not assert the INT function.	A
P3	7	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin never changes states and would not assert the INT function.	A
GND	8	Short between GND and Supply. Damage to device is not expected but may cause damage on a system level. Functionality is not guaranteed under these conditions.	B
P4	9	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin will never change states and would not assert the INT function.	A
P5	10	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin will never change states and would not assert the INT function.	A
P6	11	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin never changes states and would not assert the INT function.	A
P7	12	Worst case situation: Pin is configured to be an output LOW. A short to supply would cause high current draw to the pin due to a path from Vcc to GND. Potential damage to device may occur due to violation of absolute maximum I_{OL} parameter. Functionality may be affected if the pin is configured as an input and the controller is monitoring the INT. In the case of a short to supply, the pin never changes states and would not assert the INT function.	A
#INT	13	Damage to device may occur as the I_{oL} through the pin may exceed the absolute maximum specification for the device if #INT asserts.	A
SCL	14	Damage to device is not expected because the SCL pin of the device does not drive low (does not clock stretch). On a system level, functionality could be lost due to large V_{oL} shifts because of the large I_{oL} on the bus from the short to supply. The controller's V_{oL} may exceed the V_{iL} of the device. The large I_{oL} may also damage the controller's SCL driver if the I_{oL} is larger than what the controller is spec'd for.	B
SDA	15	Damage to device may occur as the I_{oL} through the pin may exceed the absolute maximum specification for the device when the device's SDA ACKs and when it sends data back To the controller.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{ccp}	16	If supply voltage is the same voltage as V_{ccp} then no issue is expected. If supply voltage is not the same voltage as V_{cci} and is within absolute maximum specification, then no damage is expected to the device. On a system level, high current may occur due to a short between two voltage rails. If supply voltage is larger than the absolute maximum specification for the device, damage could occur.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265