Advanced Schottky Load Management

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TEXAS INSTRUMENTS

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Introduction

As the scope of the digital integrated-circuit (IC) market broadens, the need for higher speed and lower-power-dissipation logic families increases. Texas Instruments (TI) serves this ever-expanding market by providing ICs appropriate to both a wide variety of today's applications as well as tomorrow's. The Advanced Schottky (AS) family of TTL ICs was developed by TI to handle high-speed digital applications.

The higher speed of AS devices makes possible new systems designs. However, it also increases the designer's responsibility to create an operating environment conducive to high clock rates, decreased propagation delays, and faster rise and fall times. Many designers of high-speed logic are aware of this responsibility but continue to rely on low-speed TTL design rules. The result can be less than optimal.

The purpose of this application report is to help designers of high-speed digital logic systems use AS TTL ICs. Emphasis is on managing AS loads. The major subjects covered are:

- AS waveforms
- Equivalent input/output circuits
- Transmission-line models
- Effects of fanout
- Termination
- Spatial layout
- Ground-plane effects

Waveform Characteristics Influenced by AS Loads Management

Propagation Delay

Propagation delay is the time between specific reference points on the input and output signals of a digital logic device. Typically, the trip point for a device is used as a reference point. The trip point for an AS device is 1.3 V. Thus, propagation delay for any AS device is the time between an input signal crossing 1.3 V and the associated output signal crossing 1.3 V (see Figure 1).

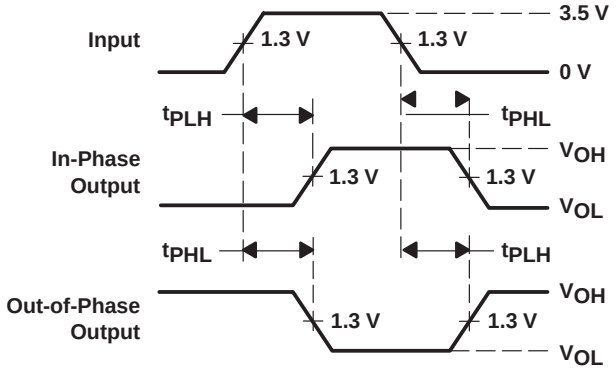
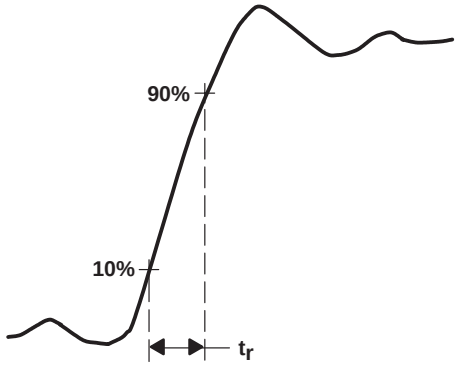


Figure 1. Definition of Propagation Delay

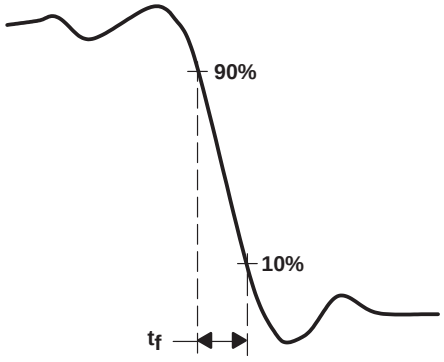
Propagation delay is a function of rise and fall times, ringing, overshoot, undershoot, line length, and fanout. It is important to create a suitable environment to produce propagation delays with acceptable values. Inadequate control of propagation delays can result in skewed signals, causing system failures. Propagation delays also determine the maximum speed of the system.

Rise and Fall Times

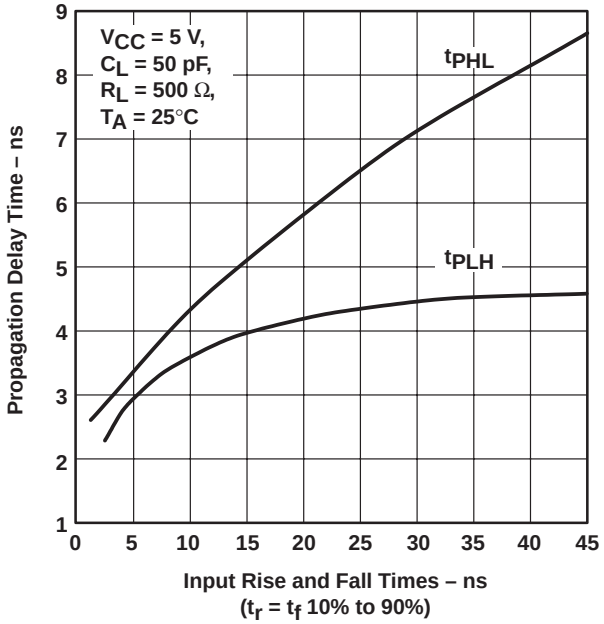
The rise time of an AS waveform (see Figure 2a) is the time a waveform takes to rise from 10% to 90% of its total voltage swing. Likewise, the fall time of an AS waveform (see Figure 2b) is the time a waveform takes to fall from 90% to 10% of its total swing. Figure 2c shows how input rise and fall times affect the propagation delay time of an 'AS804A (hex 2-input inverter). Rise and fall times are shown in Figure 2d. Figure 2 shows two interesting relationships. First, the rise and fall times are not always symmetrical. Second, advances in process technology influence rise and fall times.



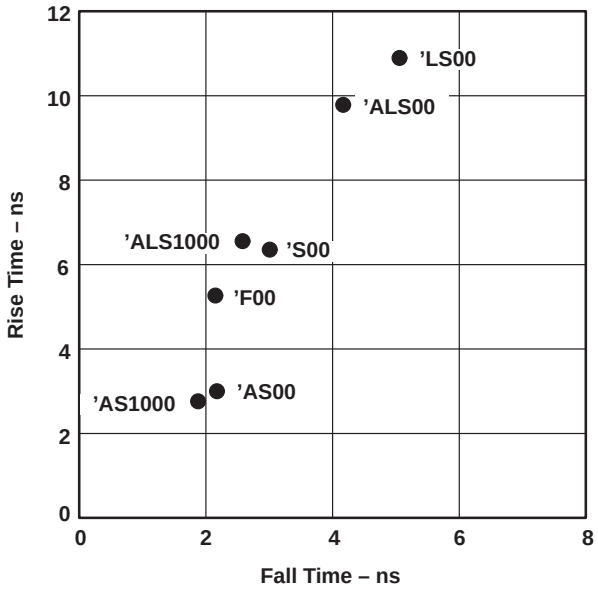
(a) RISE TIME



(b) FALL TIME



(c) PROPAGATION DELAY
AS A FUNCTION OF RISE AND FALL TIMES
('AS804)



(d) RISE AND FALL TIMES FOR TTL FAMILIES

Figure 2. Waveform Characteristics

Ringing

Ringing (in a logic circuit) is the voltage swing above and below a steady-state value occurring after a logic level transition; a typical example is shown in Figure 3. If the amplitude of the voltage swing becomes too high, a loading device may exhibit an undesired response. The bounds of ringing are defined by the maximum overshoot and undershoot values, as explained in the following paragraphs.

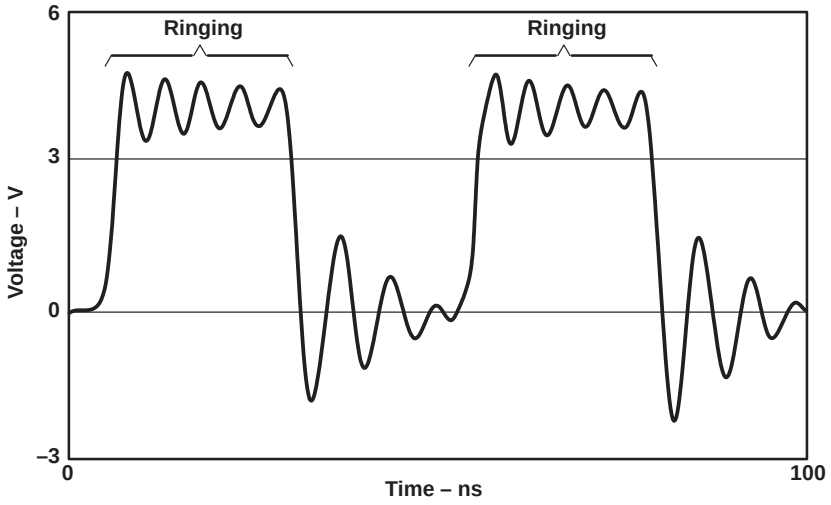


Figure 3. Ringing

Overshoot and Undershoot

In this application report, overshoot is defined as “the peak excursion beyond an expected steady-state value.” Likewise, undershoot is “the peak excursion short of an expected steady-state value.” Figure 4 illustrates these concepts.

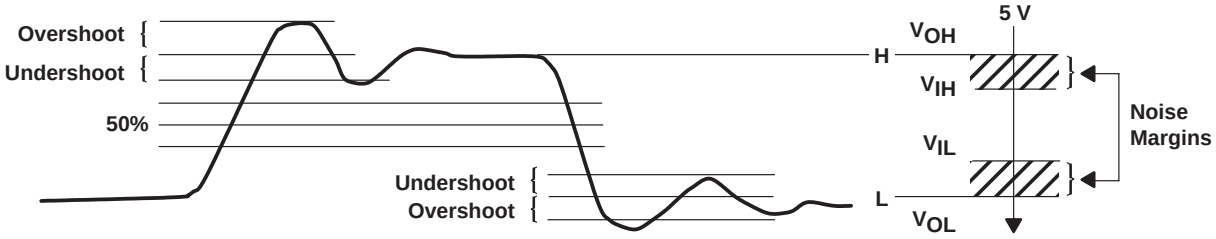


Figure 4. Overshoot and Undershoot

Referring to Figure 4, signal overshoot is defined as either the positive excursion of the signal above the logic 1 level or the negative excursion below the logic 0 level.

The effect of undershoot on the operation of a device is strongly dependent on its noise margin. The noise margin is the amount of noise that can be tolerated before the device begins to switch to a different state (see Figure 4). If the amplitude of the undershoot exceeds the noise margin, the device switches to a different state. If the amplitude of the overshoot is too great, the device may enter an invalid state (latchup) and/or require a finite time to recover before subsequent transitions can occur. The above discussion underlines the importance of minimizing overshoot and undershoot phenomena.

For AS devices, the overshoot should not exceed 35% of the logic voltage swing and undershoot should not exceed 15%. The limiting value for undershoot is determined from the noise margin of a device. Worst-case conditions are:

$V_{IL} \leq 0.8$ V
$V_{OL} \leq 0.5$ V
$V_{IH} \geq 2.0$ V
$V_{OH} \geq 2.5$ V ($V_{CC} = 4.5$ V)

Hence, the largest undershoot allowed before undesired switching would be:

$$V_{IL} - V_{OL} = 0.3 \text{ V}$$

Likewise, the worst-case logic swing for a device family is:

$$V_{OH} - V_{OL} = 2.0 \text{ V}$$

$$\text{Undershoot (max)} = \frac{0.3}{2.0} = 0.15 \text{ (15\%)}$$

The limiting value for overshoot (35%) is determined by observation.

Equivalent Circuit Models

The first step in understanding how to control a high-speed digital IC waveform emanating from an IC is to understand the circuit design. This can be achieved by constructing equivalent-circuit models. The following paragraphs break down the basic logic gate (’AS04) into input and output circuits. Later, the model is completed by connecting components and analyzing the connections.

Logic Gate

Figure 5 is a schematic of a typical AS device (’AS04). Understanding the internal operation of the gate is important, but the designer of high-speed systems should give special attention to understanding the input and output structures. These structures are used to construct a suitable model for analyzing AS-implemented systems and are explained in the following paragraphs.

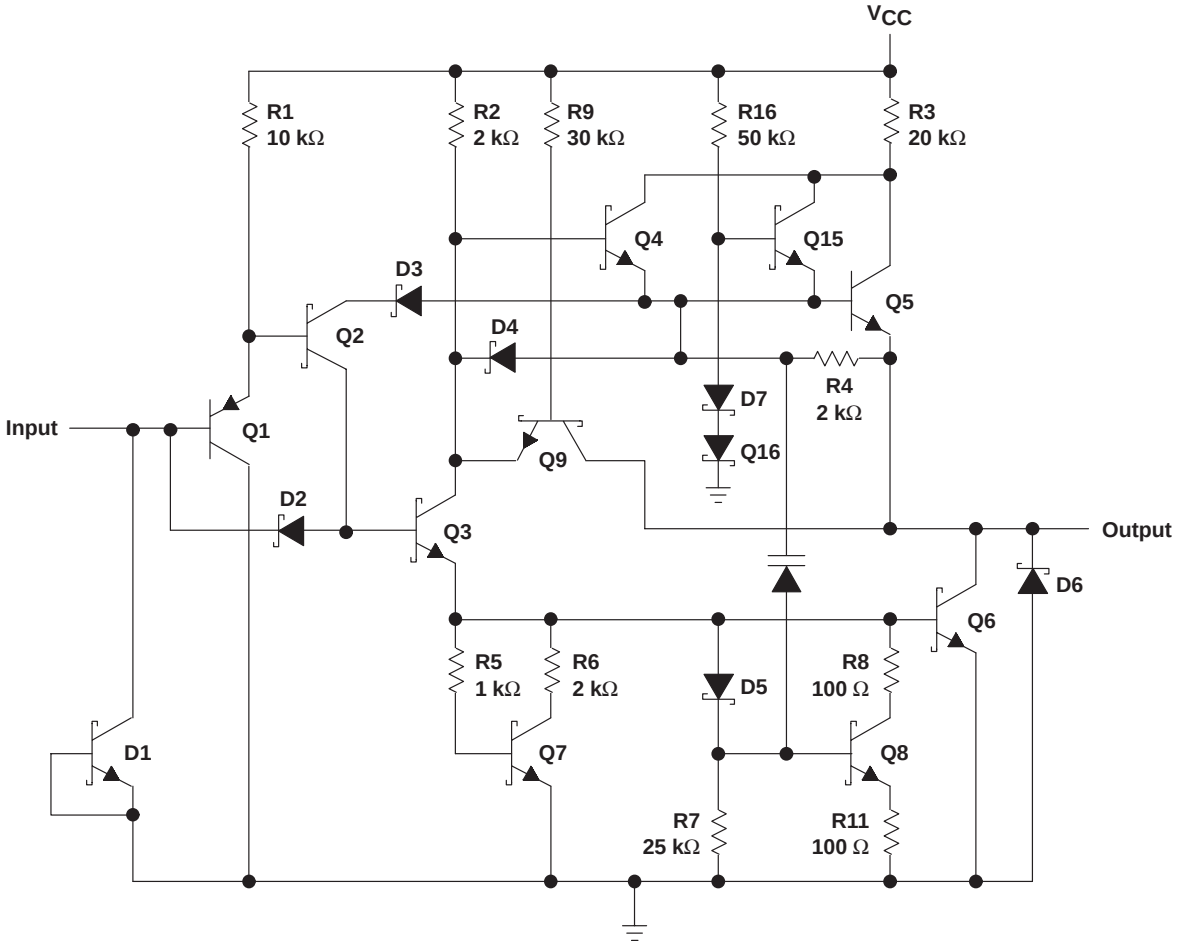


Figure 5. Schematic of ’AS04

The schematic in Figure 5 shows several features of AS gates. These features include ac *miller killers*, zero voltage clamps, ESD protection circuits, and feedback circuitry. TI uses the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to implement these features and thus achieve very fast switching times in a reduced speed-power product. Some benefits are:

- Full Schottky clamping of all saturation transistors virtually eliminates storage of excessive base charge and significantly enhances turn-off time of the transistors.
- Elimination of transistor storage time provides stable switching times across the temperature range.
- An active turnoff squares up the transfer characteristic and provides an improved high-level noise immunity.
- Input and output clamping with Schottky diodes reduces negative-going excursions on the input and outputs.
- The ion implantation process allows smaller geometries with lower parasitic capacitances, thereby decreasing switching times.
- The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

Input Equivalent

Isolating the input structure of the 'AS04 simplifies the equivalent input circuit to that shown in the schematic of Figure 6. The string of three diodes (D1, D2, and D3) and the 10-kΩ resistor simulate the loading of the input pnp transistor. D_I provides input clamping and ESD protection. When a negative potential excursion occurs, D_I turns on, clamping the signal voltage to ground. C_I and L_I correspond to the parasitic lead capacitance and inductance, respectively.

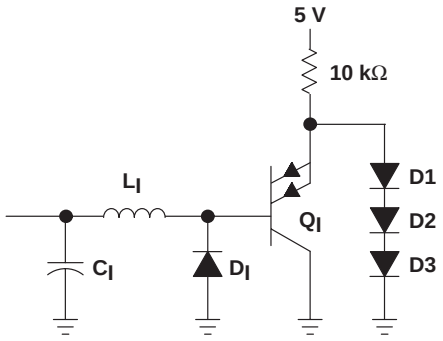
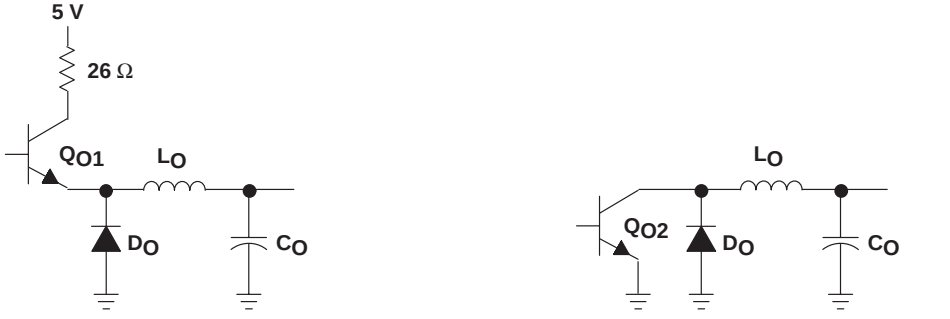


Figure 6. AS Input Structure

Output Equivalent

The output structure of the 'AS04 cannot be simplified as easily as the input structure. Unfortunately, the output impedance of AS devices is not linear or constant. Therefore, a single circuit cannot completely model the output structure. However, modeling of equivalent circuits can be based on the transition being investigated. Figure 7a shows the equivalent output circuit with a low-to-high transition, while Figure 7b shows the equivalent output circuit with a high-to-low transition. D_O simulates a zero-clamp circuit to clamp out negative-going potential excursions. C_O and L_O account for the parasitic lead impedances of the package. While Q_{O1} and Q_{O2} function basically as switches, their bipolar characteristics simulate the switching characteristics of the AS device.



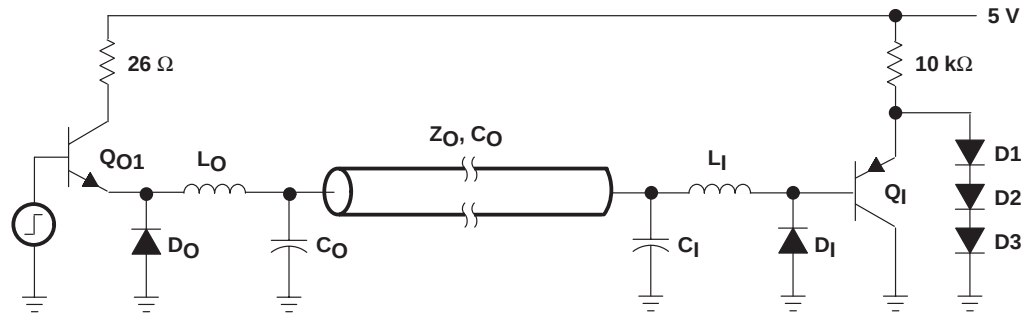
(a) LOW-TO-HIGH TRANSITION MODEL **(b) HIGH-TO-LOW TRANSITION MODEL**

Figure 7. AS Output Structure

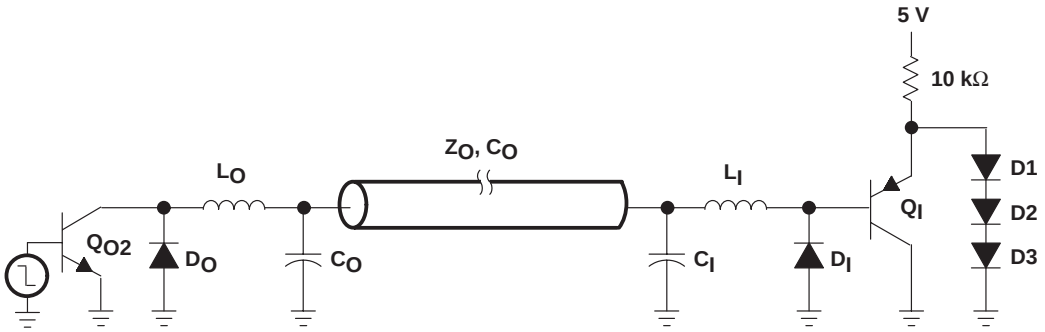
AS System Model

A combination of the equivalent circuits shown in Figures 6 and 7 can model a typical AS system (shown in Figures 8a and 8b). In these models, transmission lines connect AS devices. However, under certain circumstances any line can be modeled as a transmission line. The effects of transmission lines is discussed later.

To test the validity of the model in Figure 8, an experiment was set up comparing a computer-simulated waveform with one observed in a real environment.[1] The resulting data are in Appendix A. Briefly, there exists enough correlation to accept the models as presented in the following paragraphs.



(a) LOW-TO-HIGH TRANSITION



(b) HIGH-TO-LOW TRANSITION

Figure 8. AS System Model

Transmission Lines

Understanding the effects of transmission lines is necessary in any high-speed digital design. Any conductor can exhibit transmission-line effects if certain conditions exist. The following section describes a general model for transmission lines and provides a more detailed analysis of two types of transmission lines — microstrip lines and strip lines. It also explains the phenomenon of reflections in a transmission line and demonstrates the use of a lattice diagram to calculate total voltage at any point in a transmission line.

Transmission-Line Theory

Transmission lines may be modeled by using a distributed circuit parameter representation as shown in Figure 9. In the figure, the following definitions are used:

R_O = characteristic resistance per unit length
G_O = characteristic conductance per unit length
C_O = characteristic capacitance per unit length
L_O = characteristic inductance per unit length
dx = a unit length of transmission line

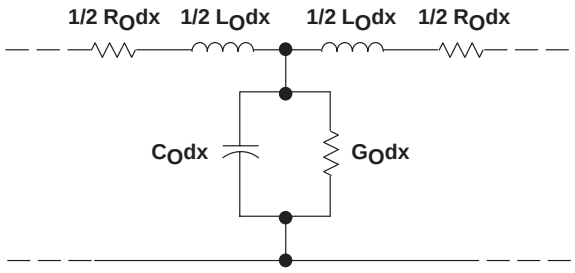


Figure 9. Transmission-Line Components

A finite length of cable can be regarded as an infinite number of differentially small circuits as shown in Figure 9. From this model, we can derive the following differential equation:

$$\frac{d^2v}{dx^2} = L_OC_O\frac{dv^2}{dt^2} + (R_OC_O + L_OG_O)\frac{dv}{dt} + R_OG_Ov \quad \textbf{(1)}$$

If the resistive and conductive components of the transmission-line model are neglected (i.e., a lossless line assumed), equation 2 results. For the scope of this analysis, this assumption is valid; the resistive and conductive components are very small, and result in very small potential differences compared to ordinary AS voltage levels.

$$\frac{d^2v}{dx^2} = L_OC_O\frac{d^2v}{dt^2} \quad \textbf{(2)}$$

The general solution of the wave equation is the impulse response of the transmission line. By convolving the impulse response with the actual input to the transmission line, the actual response to any input can be determined. A Fourier analysis provides insight into the impulse response of the transmission-line model, allowing the designer to (1) solve the wave equation, (2) perform convolution easily, and (3) study different characteristics of the resulting signal while remaining in the Fourier domain. Appendix B details the derivation of the impulse response, V(x,t).

$$V(x, t) = \delta(x - vt) \quad \textbf{(3)}$$

Where:

V(x,t) = voltage, a function of time and space
v = velocity = $\frac{1}{\sqrt{L_OC_O}}$
x = space variable ($x \geq 0$)
t = time variable ($t \geq 0$)
δ = Dirac or impulse function

Interpreting the analysis in Appendix B, the impulse response is defined to have an amplitude when x = vt, or when:

$$\frac{x}{t} = \frac{1}{\sqrt{L_OC_O}} \quad \textbf{(4)}$$

Physically, this represents an impulse traveling down the transmission line with velocity determined by the following equation:

$$v = \frac{1}{\sqrt{L_OC_O}} \quad \textbf{(5)}$$

Figure 10a shows the input signal and its associated output signal in the time domain. Figure 10b shows the input and output signals as represented in the Fourier domain.

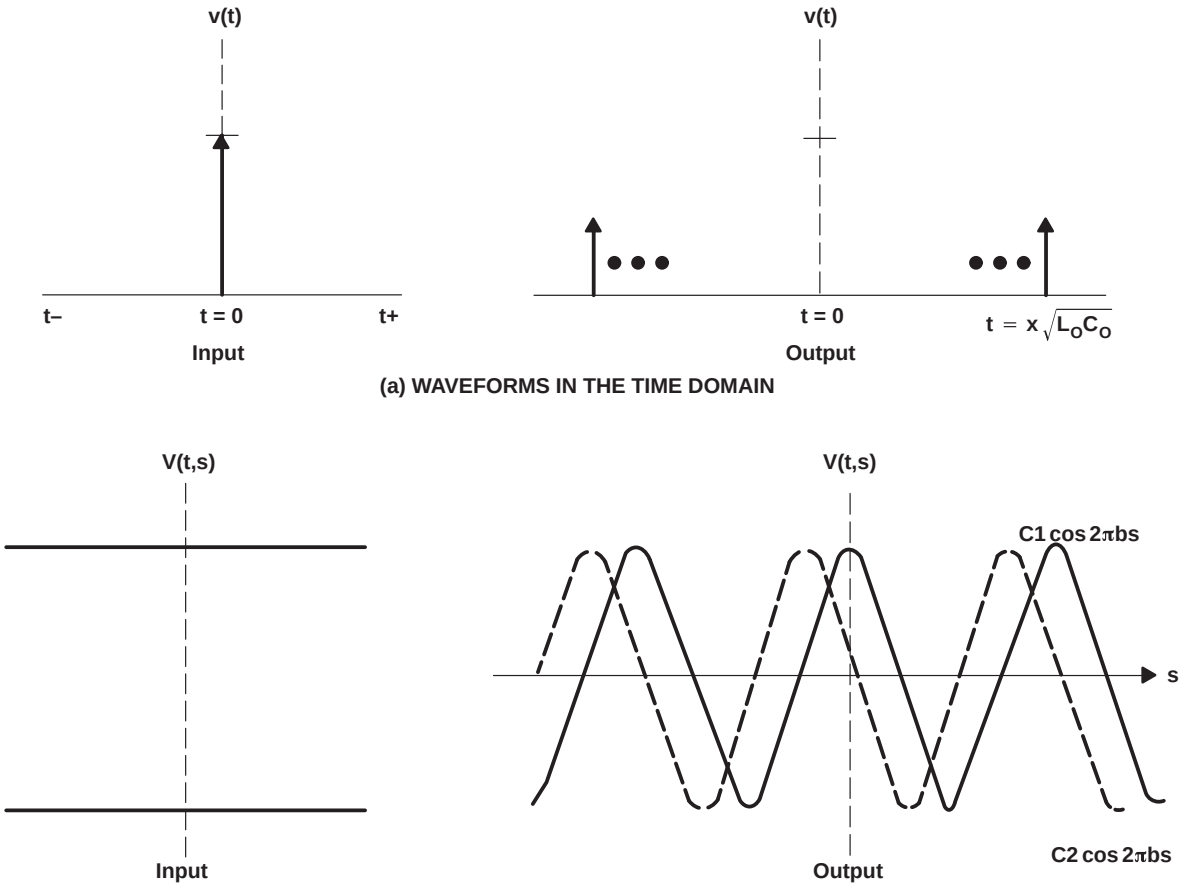


Figure 10. Waveforms in the Time and Fourier Domains

If an input signal is defined as:

$$V_s(t) = V(t)\ H(t) \quad \textbf{(6)}$$

Where:

$H(t) = 1\ (t > 0)$
$H(t) = 0\ (t < 0)$

and the impulse response is convoluted (as shown in Appendix B), the resulting signal can be solved for in the time domain:

$$V(x, t) = V(x - vt)\ H(x - vt) \quad \textbf{(7)}$$

or:

$$V(x, t) = V\left(t - xt_{pd}\right)\ H\left(t - xt_{pd}\right) \quad \textbf{(8)}$$

Where:

$$t_{pd} = \frac{1}{v}$$

The transmission line passes the signal undistorted at a velocity determined by:

$$v = \frac{1}{\sqrt{L_O C_O}} \quad \textbf{(9)}$$

An identical analysis involving current instead of voltage provides a resulting impulse response in the time domain.

Dividing the voltage response by the current response yields the characteristic impedance (Z_O).

$$Z_O = \sqrt{\frac{L_O}{C_O}} \quad \textbf{(10)}$$

The results lead to the further conclusion that given any input signal, Vs(t), the transmission line responds by passing the input delayed by:

$$t_{pd} = \sqrt{L_O C_O} \quad \textbf{(11)}$$

$$t_{pd} = Z_O C_O \quad \textbf{(12)}$$

Here, t_{pd} has units of time per unit length. If a line length of L is assumed, the actual time can be defined by the following:

$$T_{pd} = L\ t_{pd} \quad \textbf{(13)}$$

In equation 13 and the remainder of this report, the uppercase T_{pd} indicates units of time; lowercase t_{pd} indicates units of time per unit length.

Transmission-Line Types

Although many different types of transmission lines (conductors) exist, this report discusses only the two most commonly found on PC boards: microstrip lines and strip lines.

Microstrip Lines

A microstrip line consists of a signal conductor separated from a ground plane by a dielectric insulating material. The characteristic impedance of a microstrip line is given by:

$$Z_O \simeq \frac{87}{er + 1.41} \ln\frac{5.98\ H}{0.8\ W + T} \quad \text{(Blood 1983)} \quad \textbf{(14)}$$

Where:

er = relative dielectric constant of the board material (about 5 for G-10 fiberglass-epoxy boards)
W, H, T = dimensions (in mils) as indicated in Figure 11

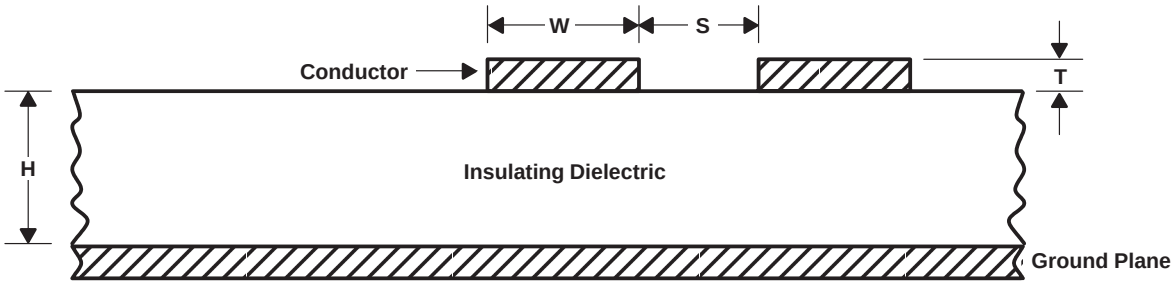


Figure 11. Microstrip-Line Structure

Equation 14 is adequate for $0.1 \le W/H \le 3.0$ and for $1 \le er \le 15$. Table 1 provides typical microstrip-line characteristics.

Table 1. Typical Microstrip-Line Characteristics

DIMENSIONS (mils)		LINE IMPEDANCE Z_O (Ω)	CAPACITANCE C_O (pF/in)
H	W		
6	20	35	3.33
6	15	40	2.92
15	20	56	2.50
15	15	65	2.17
30	20	80	1.67
30	15	89	1.50
60	20	104	1.33
60	15	113	1.17
100	20	121	1.08
100	15	130	1.00

NOTE: er = 5, T = 1.50

The propagation delay can be calculated as:

$$t_{pd} \simeq 1.017\sqrt{0.475er + 0.67} \ \ ns/ft \quad \textbf{(15)}$$

or:

$$t_{pd} \simeq 3.34\sqrt{0.475er + 0.67} \ \ ns/m \quad \textbf{(16)}$$

Using the typical value of 5 for er, the propagation delay for microstrip lines is calculated as:

$$t_{pd} \simeq 1.77 \ \ ns/ft \quad \textbf{(17)}$$

or:

$$t_{pd} \simeq 5.81 \ \ ns/m \quad \textbf{(18)}$$

Strip Lines

A strip line is a strip conductor centered in a dielectric medium between two voltage planes. The characteristic impedance is given by the following equation[1], which refers to Figure 12:

$$Z_O \simeq \frac{60}{\sqrt{er}} \ln\frac{5.98\ H}{\pi(0.8\ W + T)} \quad \textbf{(19)}$$

Equation 19 is accurate for $\frac{W}{H - T} < 0.35$ and $\frac{T}{H} < 0.25$. Table 2 provides typical strip-line characteristics.

The propagation delay for strip lines per unit length can be calculated as:

$$t_{pd} \simeq 1.017\sqrt{er} \ \ ns/ft \quad \textbf{(20)}$$

or:

$$t_{pd} \simeq 3.34\sqrt{er} \ \ ns/m \quad \textbf{(21)}$$

For G-10 fiberglass-epoxy board, the propagation delay reduces to:

$$t_{pd} \simeq 2.26 \ \ ns/ft \quad \textbf{(22)}$$

or:

$$t_{pd} \simeq 7.41 \ \ ns/m \quad \textbf{(23)}$$

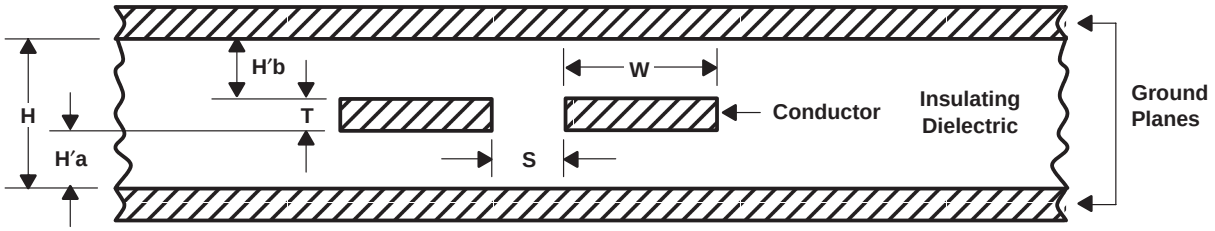


Figure 12. Strip-Line Structure

Table 2. Typical Strip-Line Characteristics

DIMENSIONS (mils)		LINE IMPEDANCE Z_O (Ω)	CAPACITANCE C_O (pF/in)
H	W		
6	20	27	6.67
6	15	32	5.83
10	20	34	5.58
10	15	40	4.67
12	20	37	4.75
12	15	43	4.00
20	20	44	4.00
20	15	51	3.50
30	20	55	3.25
30	15	61	2.92

NOTE: er = 5, T = 1.50, H′a = H′b

Reflections

If a load, Z_L, exists on a transmission line such that $Z_L \neq Z_O$, a waveform reflects into the transmission line upon encountering the load. The magnitude of reflection is normally defined by a reflection coefficient. The reflection coefficient (Γ) at the load is derived by use of Ohm's Law. If V_i is the incident voltage and V_r is the reflected voltage, the following equation must be true at node B of Figure 13:

$$V_i + V_r = \left(\frac{V_i}{Z_O} - \frac{V_r}{Z_O}\right)Z_L \quad \textbf{(24)}$$

Therefore, Γ, defined as $\frac{V_r}{V_i}$ is:

$$\Gamma_{load} = \frac{Z_{load} - Z_O}{Z_{load} + Z_O} \quad \textbf{(25)}$$

Likewise,

$$\Gamma_{source} = \frac{Z_{source} - Z_O}{Z_{source} + Z_O} \quad \textbf{(26)}$$

The amount of reflection voltage (V_r) is given by V_i, the voltage incident at the point of reflection.

The model of the transmission line can now be completed. In Figure 13, the voltage seen at point A is given by equation 27:

$$V_a = V_S \frac{Z_O}{Z_O + Z_S} \quad \textbf{(27)}$$

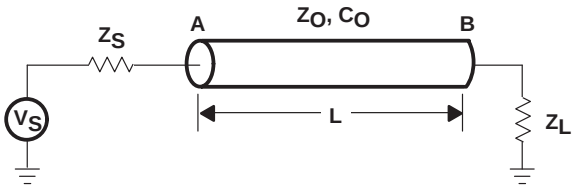


Figure 13. Loaded Transmission Line

Then V_a enters the transmission line and appears at point B delayed by T_{pd}.

$$V_b = V_a(x - vt)\ H(x - vt) \quad \textbf{(28)}$$

For equation 28, x is the distance along the transmission line from point A. The waveform then encounters the load Z_L, and a reflection can occur. The reflected wave enters the transmission line at point B and appears at point A T_{pd} (or L t_{pd}) later.

$$V_{r1} = \Gamma_{load} V_b \quad \textbf{(29)}$$

The process continues indefinitely.

$$V_{r2} = V_{r1}\Gamma_{source} \quad \textbf{(30)}$$

If each reflected waveform is treated as a separate source, dependent on the reflection coefficient at that end and the incident waveform, superposition can be applied to develop equation 31, which describes the waveform seen at any point on the transmission line at any given time.

$$\begin{aligned} V(x,t) = {} & \frac{Z_O}{Z_O + Z_S}[V(x - vt)]\ [H(x - vt)] \\ & + \Gamma_l\{V[x - (2L + vt)]\}\ \{H[x - (2L + vt)]\} \\ & + \Gamma_l\Gamma_s\{V[x - (2L - vt)]\}\ \{H[x - (2L - vt)]\} \\ & + \Gamma_l\Gamma_s\{V[x - (4L - vt)]\}\ \{H[x - (4L - vt)]\} \\ & + \Gamma_l^{\,2}\,\Gamma_s^{\,2}\{V[x - (4L + vt)]\}\ \{H[x - (4L + vt)]\} + \ldots \end{aligned} \quad \textbf{(31)}$$

Each reflection is added to the total voltage through the unit step function, H(t). Alternately, equation 31 can be rewritten as:

$$\begin{aligned} V(x,t) = {} & \frac{Z_O}{Z_O + Z_S}\left[V\left(t - t_{pd}x\right)\right]\ \left[H\left(t - t_{pd}x\right)\right] \\ & + \Gamma_l\left\{V\left[t - t_{pd}(2L - x)\right]\right\}\ \left\{H\left[t - t_{pd}(2L - x)\right]\right\} \\ & + \Gamma_l\Gamma_s\left\{V\left[t - t_{pd}(2L + x)\right]\right\}\ \left\{H\left[t - t_{pd}(2L + x)\right]\right\} \\ & + \Gamma_l\Gamma_s\left\{V\left[t - t_{pd}(4L - x)\right]\right\}\ \left\{H\left[t - t_{pd}(4L - x)\right]\right\} \\ & + \Gamma_l^{\,2}\,\Gamma_s^{\,2}\left\{V\left[t - t_{pd}(4L + x)\right]\right\}\ \left\{H\left[t - t_{pd}(4L + x)\right]\right\} + \ldots \end{aligned} \quad \textbf{(32)}$$

With this equation, the potential now can be followed along any point of the transmission line in time. Thus, the model for an entire system has been completed.

Lattice Diagrams

The lattice diagram is a convenient tool for calculating the total voltage as described by equations 31 and 32. Two vertical lines are drawn to represent points A and B on the horizontal dimension, x. The vertical dimension then represents time. Thus, a waveform travels back and forth between points A and B in time, producing the lattice diagram shown in Figure 14. The voltage at a given point can be calculated as the sum of all the individual reflected voltages up to that time. Notice that at each discontinuity, two waves are converging: the incident wave and the reflected wave. Therefore, the voltage at the endpoints A or B at the time of the waveform reflection would be calculated by summing both the incident and reflected waves up to and including the point in question.

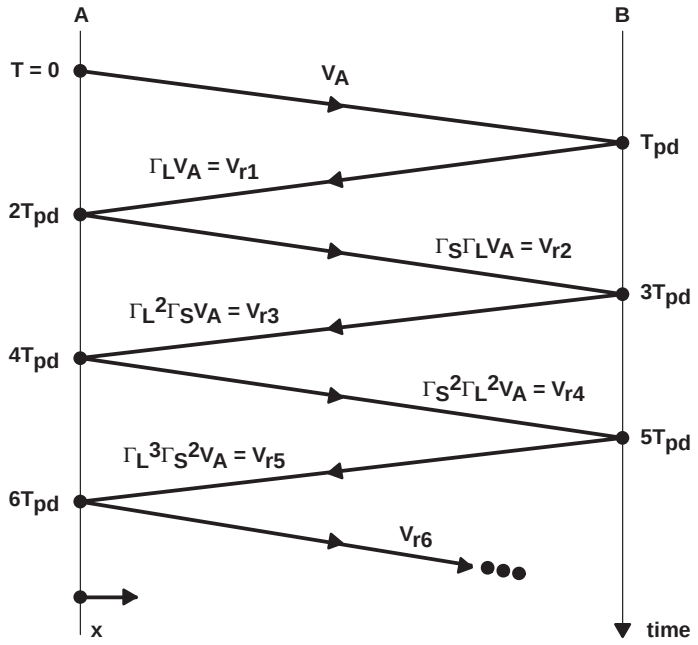


Figure 14. Lattice Diagram

As an example, let the simple configuration shown in Figure 13 be assumed. Let $R_S = 30\ \Omega$ (a typical high-state AS source impedance) and let $R_L = 100\ \Omega$ (arbitrarily). Finally, let $Z_O = 75\ \Omega$. The appropriate reflection coefficients can be calculated as:

$$Z_O = 75\ \Omega$$
$$Z_{source} = 30\ \Omega$$
$$Z_{load} = 100\ \Omega$$

$$\Gamma_{source} = \frac{30 - 75}{30 + 75} = -0.42857$$
$$\Gamma_{load} = \frac{100 - 75}{100 + 75} = 0.14286$$

$$V_S = 3.70000\ V$$
$$V_a = V_s \frac{75}{75 + 30} = 2.64286\ V$$
$$V_{r1} = 2.64286 \times 0.14286 = 0.37755\ V$$
$$V_{r2} = 0.37755 \times -0.42857 = -0.16181\ V$$
$$V_{r3} = -0.16181 \times 0.14286 = -0.02312\ V$$
$$V_{r4} = -0.02312 \times -0.42857 = 0.00991\ V$$
$$V_{r5} = 0.00991 \times 0.14286 = 0.00142\ V$$
$$V_{r6} = 0.00142 \times -0.42857 = -0.00061\ V$$
$$V_{r7} = -0.00061 \times 0.14286 = -0.00009\ V$$

Thus, the voltage at point B can be tabulated as shown in Table 3. The corresponding lattice diagram is shown in Figure 15.

Table 3. Voltage at End Points A and B

T_{pd}	V(A,t)	V(B,t)
0	2.64286	0
1	2.64286	3.02041
2	2.85860	3.02041
3	2.85860	2.83549
4	2.84539	2.83549
5	2.84539	2.84681
6	2.84620	2.84681
7	2.84620	2.84611

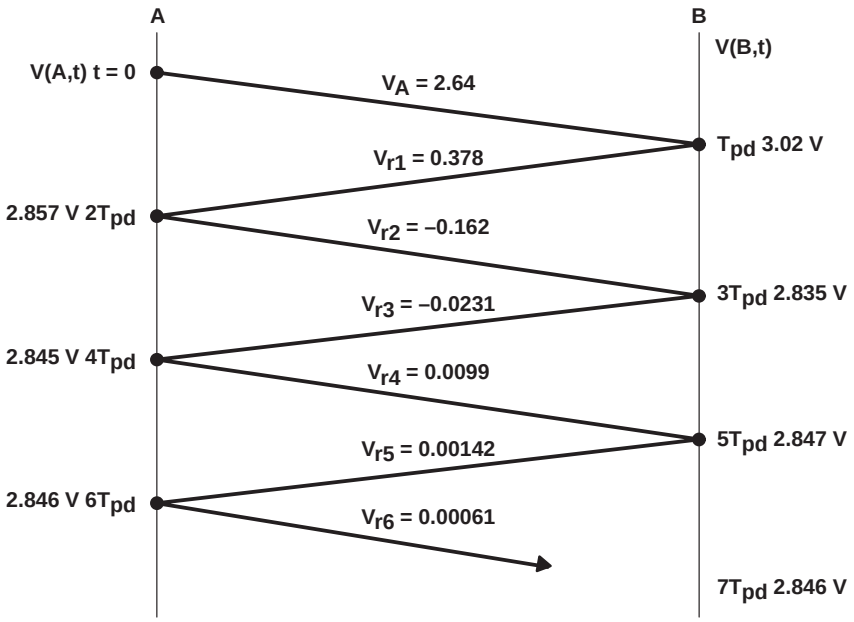


Figure 15. Lattice Diagram Example

Fanout

The fanout of a device is defined as the number of other devices it can drive. While the fanout of a device is specified by the manufacturer, the effects of fanout on the waveform of a device are not. Fanout affects the transmission-line model, the propagation delay as seen by the system, the rise and fall times of system waveforms, and the proposed solutions to control overshoot and undershoot. Therefore, it is important that these effects be kept in mind.

Influence on Transmission-Line Model

A device driving more than one other device is said to have a fanout of more than one. The configuration of the loading devices is important. If the loading devices are all lumped at the end of the transmission line (see Figure 16 for lumped loading), the transmission model developed above is still valid. However, a correction is required because of the excess capacitance at the load.[2] This correction is also dependent on the type of termination scheme, as discussed in the following paragraphs.

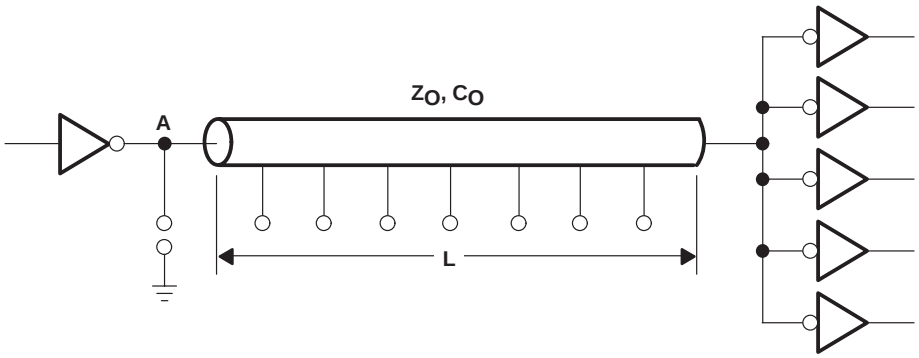


Figure 16. Transmission Line With Lumped Loading

If the loading devices are approximately equally spaced along the length of the transmission line, the model must be altered regardless of the termination scheme.

The input equivalent models of AS devices discussed above show that the impedance of a loading device is very high and can be considered here as purely capacitive. This is especially true when AS devices operate at high speeds. Therefore, each load is seen by the driving device as a capacitor, C_n, to ground. If the loads are distributed evenly, d inches apart, the characteristic capacitance (C_O) is increased from C_O to $C_O + C_d$, where C_d is C_n/d.

$$Z_O = \sqrt{\frac{L_O}{C_O + C_d}} \quad \textbf{(33)}$$

and:

$$t_{pd} = \sqrt{L_O(C_O + C_d)} \quad \textbf{(34)}$$

or:

$$t_{pd}(new) = t_{pd}(old)\sqrt{1 + \frac{C_d}{C_O}} \quad \textbf{(35)}$$

Equations 34 and 35 clearly show that the propagation delay of the waveform on the transmission line increases, that is, the velocity of the propagating signal decreases as each load is added to the line.

Influence on Rise and Fall Times

The rise and fall times of a signal are also affected by fanout, both adversely (for both lumped and distributed loads). Yeargan[1] treats the output waveform (V_O) as an exponential with a time constant defined by R_S and C_{eq}:

$$V_O = V\left(1 - \exp\frac{-t}{R_S C_{eq}}\right) \quad \textbf{(36)}$$

Where:

$C_{eq} = C_O = nC_n$
R_S = output impedance of the driving gate
n = number of loads on the transmission line

If the rise time is defined as stated previously, solve for t_r:

$$t_r = R_S \times C_{eq}\left(\ln\frac{0.9\ v}{v} - \ln\frac{0.1\ v}{v}\right) \quad \textbf{(37)}$$

or:

$$t_r = 2.2\ R_S C_{eq} \quad \textbf{(38)}$$

Equations 37 and 38 show how t_r is affected by additional loads. A similar analysis provides the same relation for fall times.

The circuit in Figure 17 was used in experimental observation to confirm the effects of fanout on rise and fall times.[1] Figure 18 shows the results of this experiment at the input and output of the transmission line.

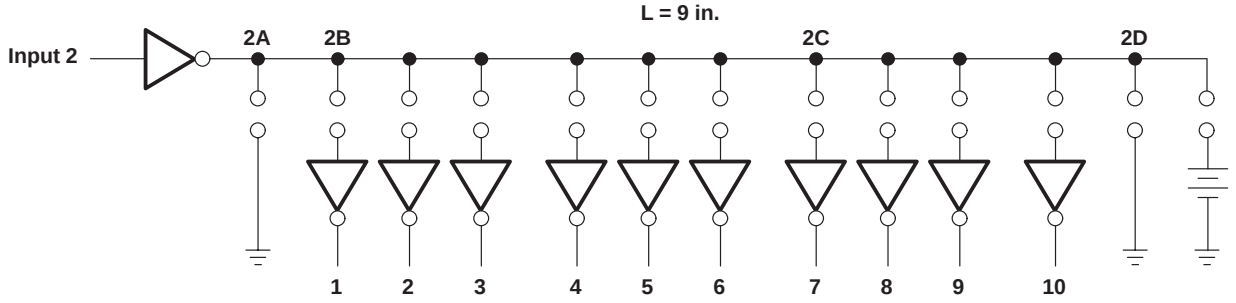


Figure 17. Schematic Diagram of a Distributed Loaded System

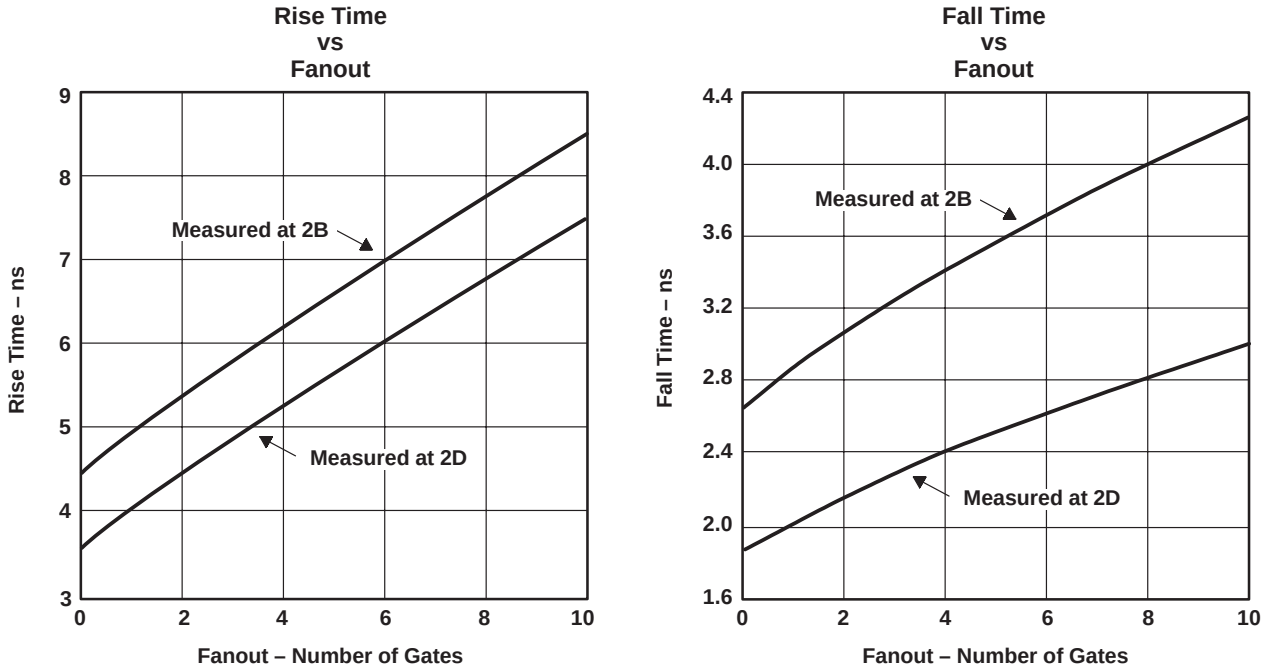


Figure 18. Rise Time and Fall Time Versus Fanout

Combined Effects on Propagation Delay

As stated previously, propagation delay is a function of rise and fall times, as well as the characteristic impedance of the transmission line. If both are affected by fanout (distributed loads), the propagation delay of these factors is also affected. The experimental circuit shown in Figure 17 confirms this effect on propagation delay.[1] Figure 19 plots the relationship of propagation delay and fanout.

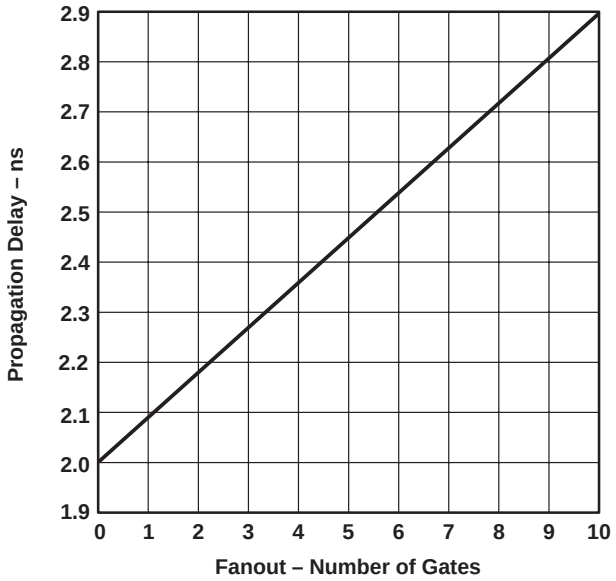


Figure 19. Propagation Delay Versus Fanout

Influence on Ringing

Finally, fanout influences the overshoot and undershoot characteristics of the waveform. That is, overshoot and undershoot are dependent on the characteristic impedance of the transmission line. Figure 20 shows an example of a waveform derived from the lattice diagram example in Figure 15. The lattice diagram shows how the waveform reacts with the reflection coefficients, which are dependent on Z_O. Overshoot is very dependent on Γ_{load}.

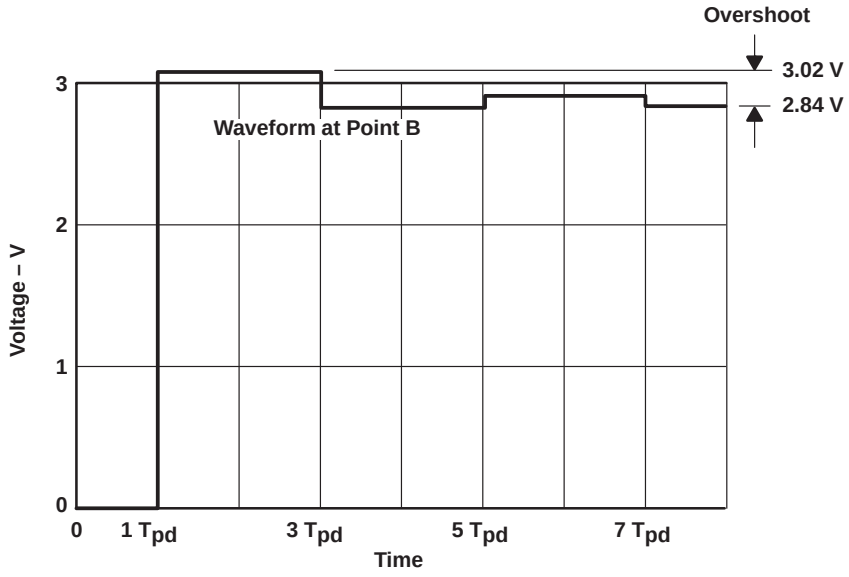


Figure 20. Waveform Derived From Lattice Example

Figure 21 shows the influence of fanout on overshoot in the test circuit of Figure 17. As fanout increases, Z_O decreases, Γ_{load} decreases, and overshoot decreases. If the reflected overshoot decreases, the subsequent undershoot decreases as well.

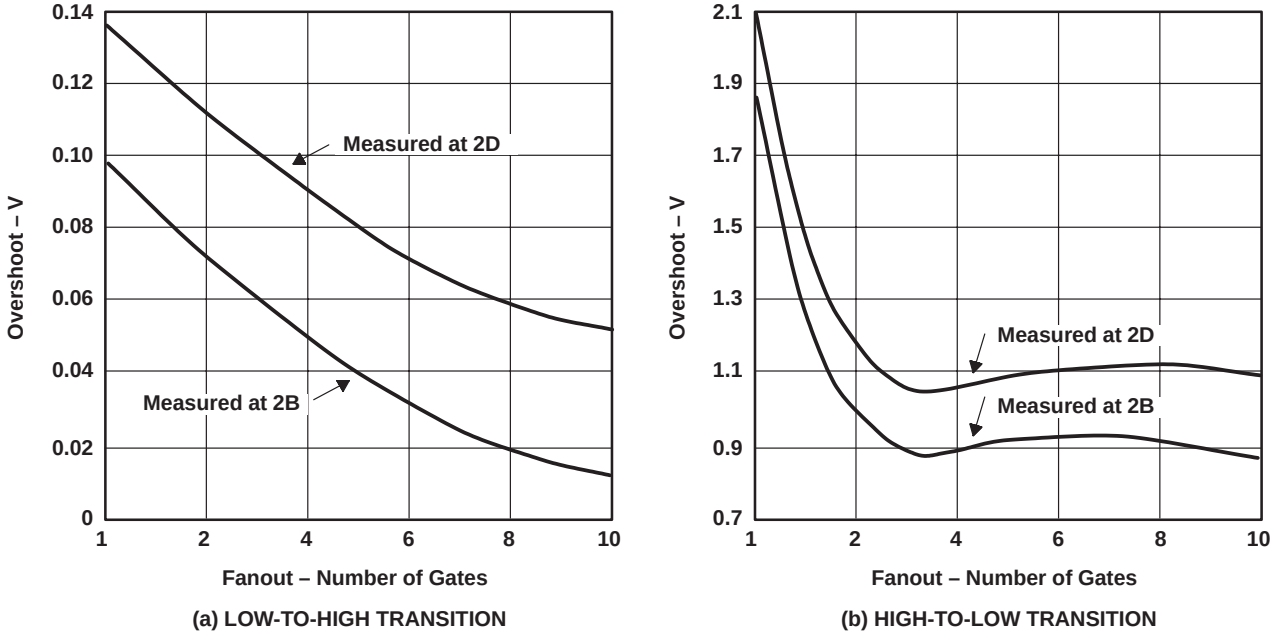


Figure 21. Overshoot Versus Fanout

Termination

When Termination is Needed

The preceding analysis and derivations can be used to predict how a signal reacts to certain environments. Figure 22 shows an unterminated line with a single load.

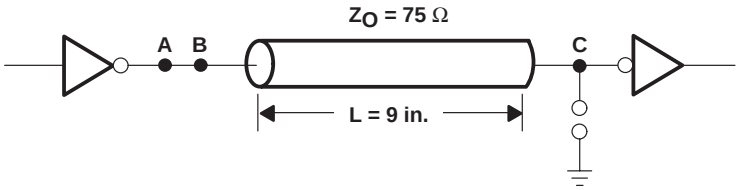


Figure 22. Unterminated Single Load

The waveform of the circuit in Figure 22 is shown in Figure 23. Initially, the input waveform travels down the transmission line with the velocity that was derived in equation 4. Assuming the line is sufficiently long, when the waveform reaches point C it encounters the unterminated load. Because the input impedance of the receiving device is very high compared to the characteristic impedance of the transmission line, Γ_{load} approaches one, sending the entire signal V_O back to the source and resulting in a large overshoot. The signal proceeds toward point A where Γ_s (negative) produces a negative-going reflection, thus creating a substantial undershoot (dependent on the value of R_S). This successive overshoot and undershoot continues, and the phenomenon of ringing occurs.

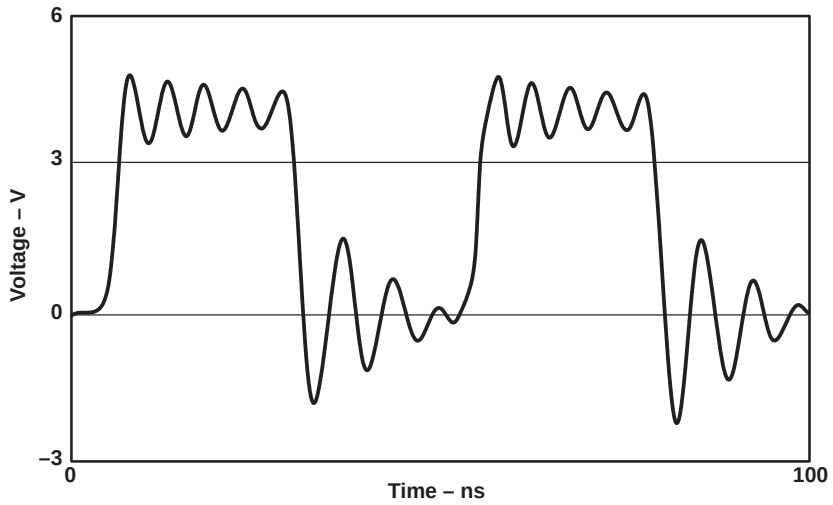


Figure 23. Unterminated Single-Load Waveform

If the line is sufficiently short, reflections are part of the rise time of the signal. Being part of the rise or fall time, the reflections do not contribute to overshoot or undershoot. Hence, if the length of the transmission line is shorter than l_{max} (see equation 39), overshoot and undershoot are held to less than 15% of the logic swing.[3]

$$l_{max} \leq \frac{t_r}{2t_{pd}} \quad \textbf{(39)}$$

Where:

t_r = rise time of the signal
$t_{pd} = Z_O C_O$

and:

Z_O = characteristic line impedance
C_O = equivalent capacitance per unit length of the line

If the line is longer than l_{max}, termination is required to reduce overshoot and undershoot (i.e., ringing). Table 4 is a good guide to deciding when termination is needed. It shows the longest unterminated length of transmission line, given its characteristics and the fanout. The values are derived from the preceding analysis and are observed to be approximately correct. It is important to reduce these values by 10% for added margin.

Table 4. Maximum Line Length Without Termination

FANOUT	1	2	4	8	Z_O (Ω)
C_{pd} (pF)	4.70	9.40	18.80	37.60	
Microstrip 0.15 t_{pd} (ns/in)† (maximum length in inches)	9.37	8.67	7.45	5.61	50
	9.11	8.20	6.70	4.68	68
	9.01	8.03	6.44	4.38	75
	8.92	7.86	6.19	4.12	82
	8.81	7.67	5.92	3.85	90
	8.67	7.45	5.61	3.55	100
Strip 0.19 t_{pd} (ns/in)† (maximum length in inches)	7.38	6.83	5.86	4.42	50
	7.17	6.46	5.27	3.68	68
	7.10	6.32	5.07	3.45	75
	7.02	6.19	4.87	3.24	82
	6.93	6.04	4.66	3.03	90
	6.83	5.86	4.42	2.79	100

† t_r = 4 ns

Resistive Termination

Overshoot and undershoot caused by incorrect length of the transmission line can be reduced to tolerable levels by the correct choice of termination.

Parallel Termination

Parallel termination is achieved by placing a resistor of appropriate value to ground at the input of the loading device, as shown in Figure 24. Because the input impedance of the device is high compared to the characteristic line impedance, the resistor and device in parallel function as a single impedance, with magnitude defined by the resistor. When the resistor matches the line impedance, the reflection coefficient at the load, Γ_{load}, approaches zero and no reflection occurs. The termination should be placed as close to the loading device as possible.

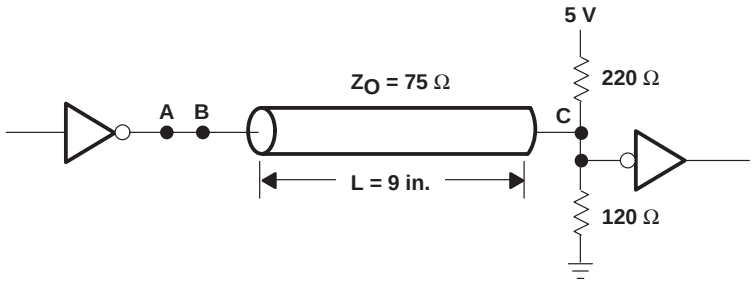


Figure 24. Parallel Termination

Blood[2] highlights an important feature of parallel termination: an undistorted waveform along the entire line. Another feature is that loading a long line (fanout greater than one, lumped at the end of the line) while using parallel termination does not affect rise and fall times or the propagation delay of the driving device. Figure 25 shows the waveforms observed from the transmission line in Figure 24 with parallel termination.

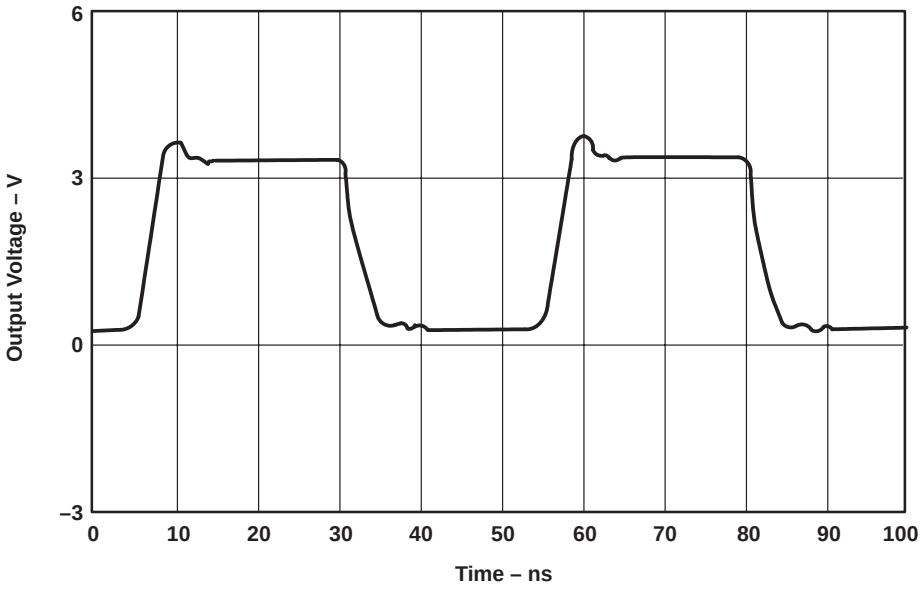


Figure 25. Parallel-Termination Waveform

Series Termination

Ringing on longer lines may also be controlled by using a series termination technique. Series termination is accomplished by putting a resistor in series with the transmission line at the driving device. This is also known as series damping. The value of the resistor plus the impedance looking into the driving device should approximate the impedance of the transmitting line as closely as possible. When this condition is obtained, the reflection coefficient at the source goes to zero and the ringing is damped out. See Figure 26 for an example of series termination.

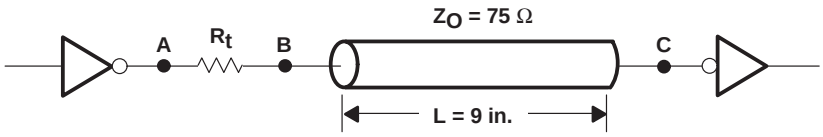


Figure 26. Series Termination

At t0, the voltage at point A is V_S. The voltage at point B (at t0+) is given by equation 40:

$$V_b = V_a \frac{Z_O}{R_t + R_S + Z_O} \quad \textbf{(40)}$$

$$V_b = \frac{V_a}{2} \quad \textbf{(41)}$$

Half the signal is propagated to the load, whose reflection coefficient sends the entire signal back into the transmission line, effectively doubling the signal.

$$V_{rl} = V_b \quad \textbf{(42)}$$

$$V\left(x, T_{pd}+\right) = V_b + V_{rl} = V_a \quad \textbf{(43)}$$

The zero-reflection coefficient at the source prevents further reflections, thereby leaving the value of the voltage on the transmission line at the desired potential.

Series termination requires no additional power supplies, making it an attractive alternative to parallel termination schemes. However, the designer should not use distributed loading because, as shown in Figure 27, the waveforms are not undistorted along the entire length of the line.[2] Instead, lumped loading can be used with any number of loading devices at the receiving end. In this and all cases, the designer should always be sure the driving gate can supply enough current for its application and to ensure proper V_{OH} and V_{OL} levels on the line. Figure 28 shows the waveform of the circuit shown in Figure 26.

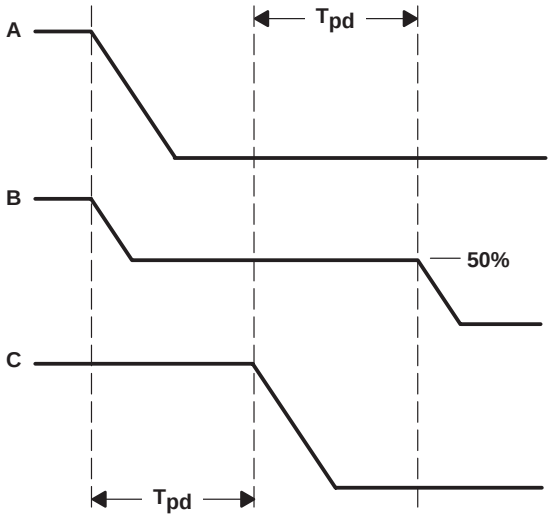


Figure 27. Relation of Series-Termination Waveforms

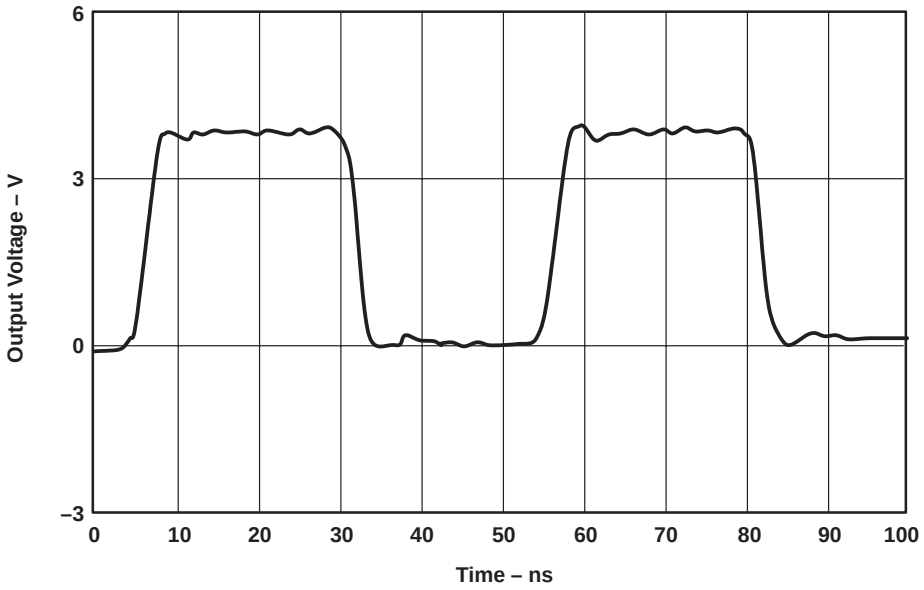


Figure 28. Series-Termination Waveform

Series termination does affect the propagation delay of a loaded system. In fact, a system with series termination experiences twice the loading effect than a system with parallel termination.[2] That is, when lumped loading is present, the increase in rise and fall times of the signal increases the propagation delay. Again, series termination is appropriate only for fanouts of one or more (lumped at the end of the line). However, as the fanout increases, the propagation delay of the waveform increases.

Fanout Correction

The propagation delay for lumped loads requires a correction and is dependent on the type of termination used. The correction is:

For series termination:

$$t_{pd} = Z_O C_O + 0.7 Z_O C_T \quad \textbf{(44)}$$

For parallel termination:

$$t_{pd} = Z_O C_O + 0.35 Z_O C_T \quad \textbf{(45)}$$

Where:

Z_O = characteristic impedance as developed in previous paragraphs
C_T = total capacitance due to lumped load only

Diode Termination

The parallel and series terminations previously discussed are passive. However, power-supply constraints often lead the designer to use diodes as a termination alternative. This technique is called active termination.

Two Schottky diodes placed as shown in Figure 29 effectively reduce ringing. Several advantages are gained by this use of active termination[2]:

- No matched-impedance strip lines are required.
- No line-matching termination resistors are required.
- All overshoots, undershoots, or external noise are clamped to safe voltage-excursion levels.
- The total cost of layout can be less than with resistors because no precise transmission-line environment is necessary.
- If ringing is a problem on a line during system checkout, diode termination can be used to improve the waveform.
- Where line impedances are not well defined, as in breadboarding or prototype construction of systems using AS, use of diode termination is convenient and cost effective.

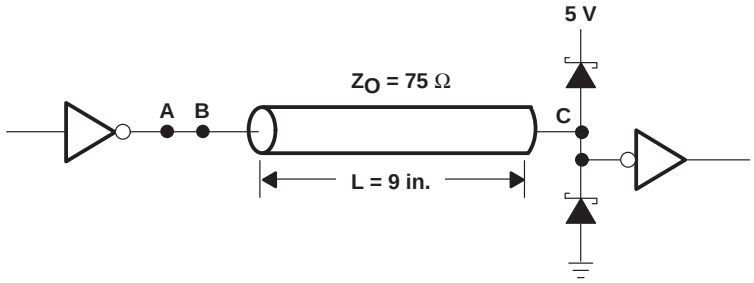


Figure 29. Active Termination

Observed waveforms of the circuit shown in Figure 29 are shown in Figure 30. Comparison of Figures 23 and 30 shows the effect of the diodes — ringing, though still present, is now within the acceptable noise margin.

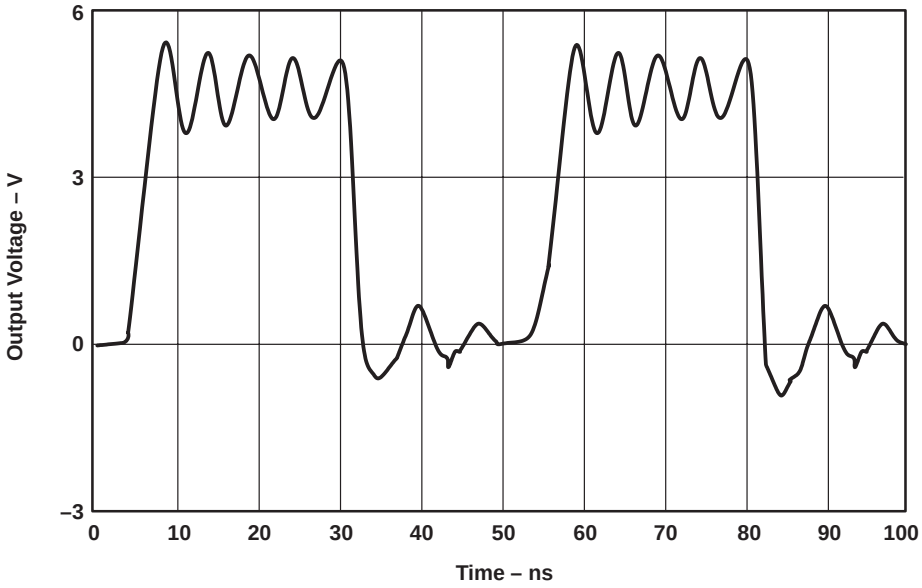


Figure 30. Active-Termination Waveform

Spatial Considerations

In very-high-speed applications, spatial considerations become very important. It has been demonstrated that the lengths of the transmission lines determine when termination is required. Therefore, these lines should be as short as possible. Any required termination — parallel-resistive, series-resistive, or diode — must be located as close to the device as possible.

In addition to the effects of line length, square corners on lines can also have an adverse effect on the system.[2] Blood[2] observed a 7.5% increase in reflection amplitude when using square rather than rounded corners. However, experiments show that the bending of runs does not seem to cause any significant signal degradation in AS systems.[1] The circuits in Figures 31 and 32 were used to establish these observations.

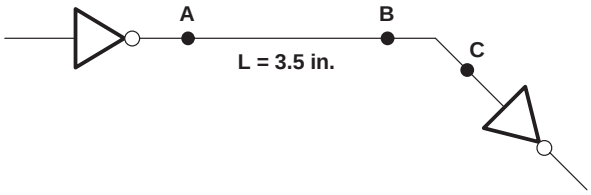


Figure 31. Circuit to Observe the Effects of a 45-Degree Bend

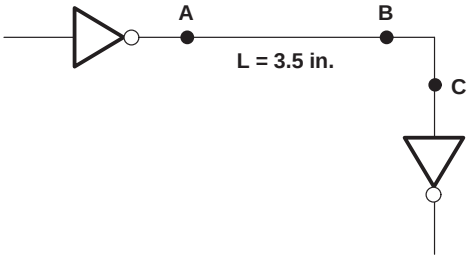
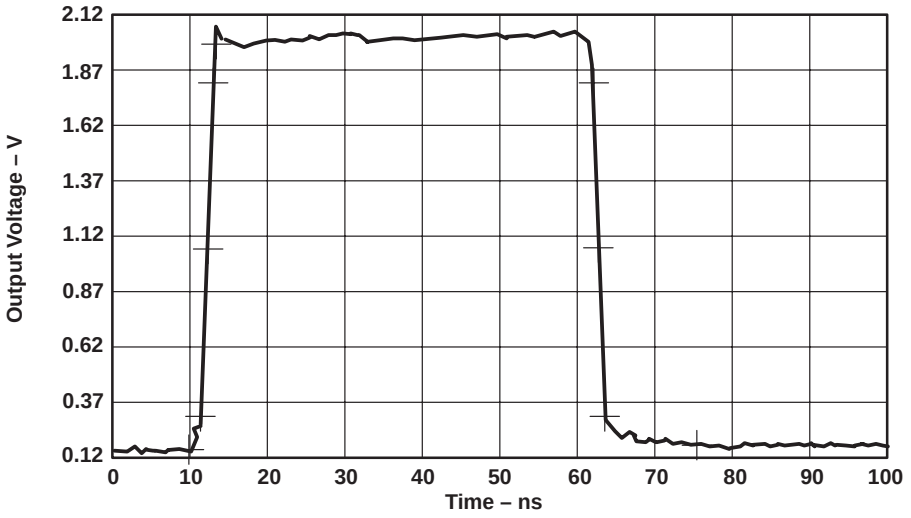


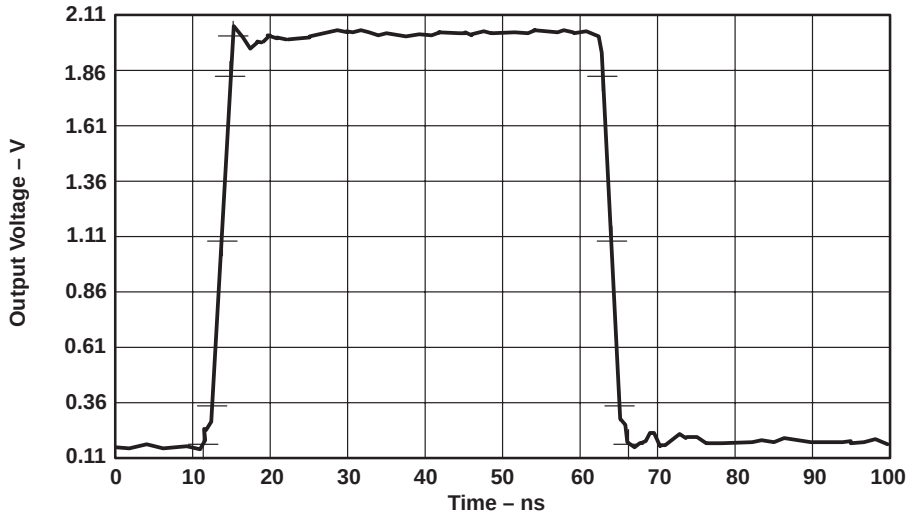
Figure 32. Circuit to Observe the Effects of a 90-Degree Bend

Ground-Plane Effects

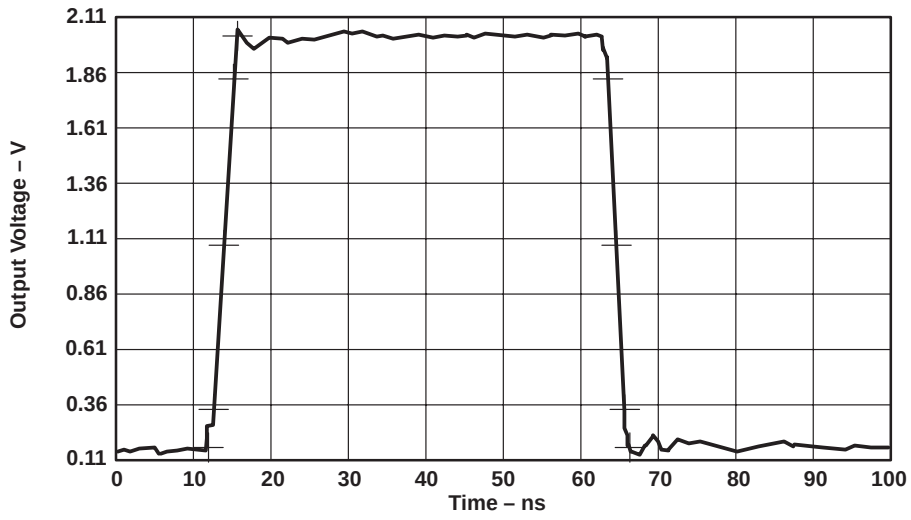
Ground planes are beneficial to the system designer and have three advantages worthy of mention. First, ground planes provide constant (well-behaved) characteristic impedances on signal conductors, as evident with strip and microstrip conductors. Second, ground planes provide a low-inductance path for ground currents on the V_{CC} supply.[2] Finally, ground planes are also beneficial in the reduction of crosstalk noise between transmission lines.



(a) WAVEFORMS AT TEST POINT A

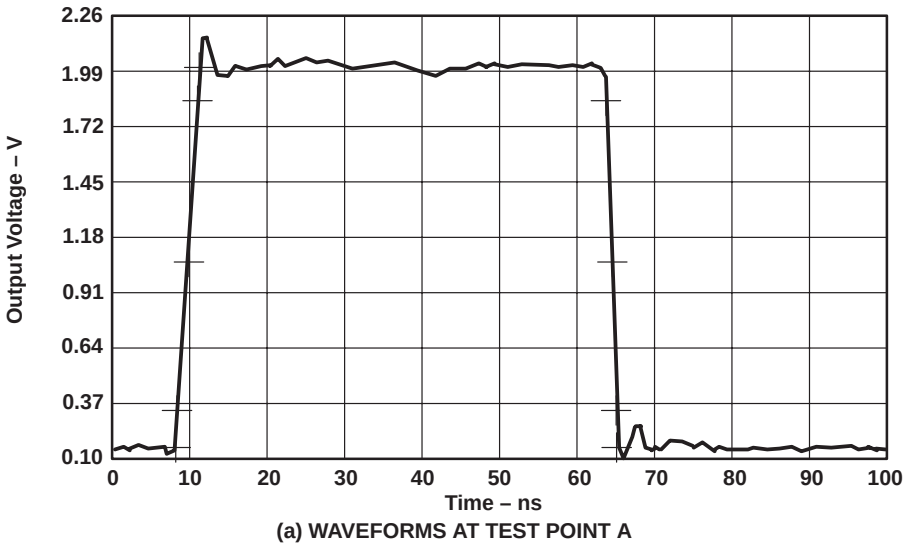


(b) WAVEFORMS AT TEST POINT B

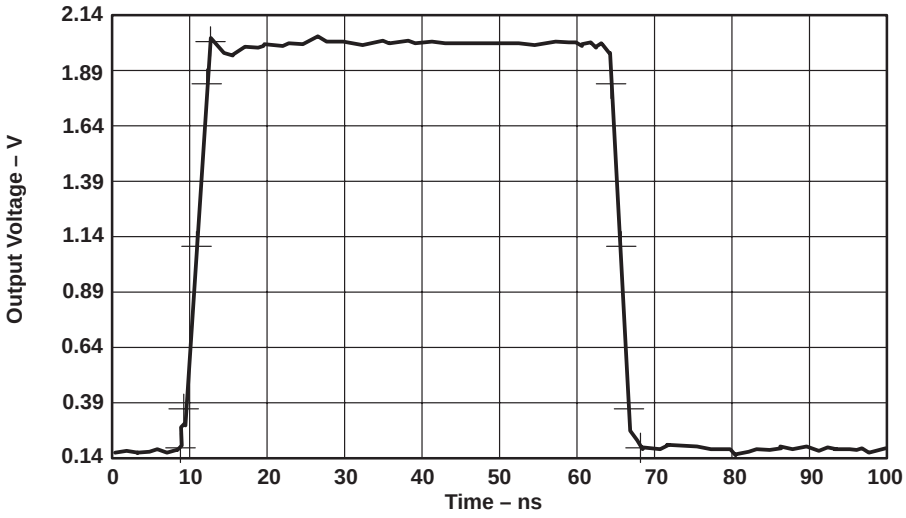


(c) WAVEFORMS AT TEST POINT C

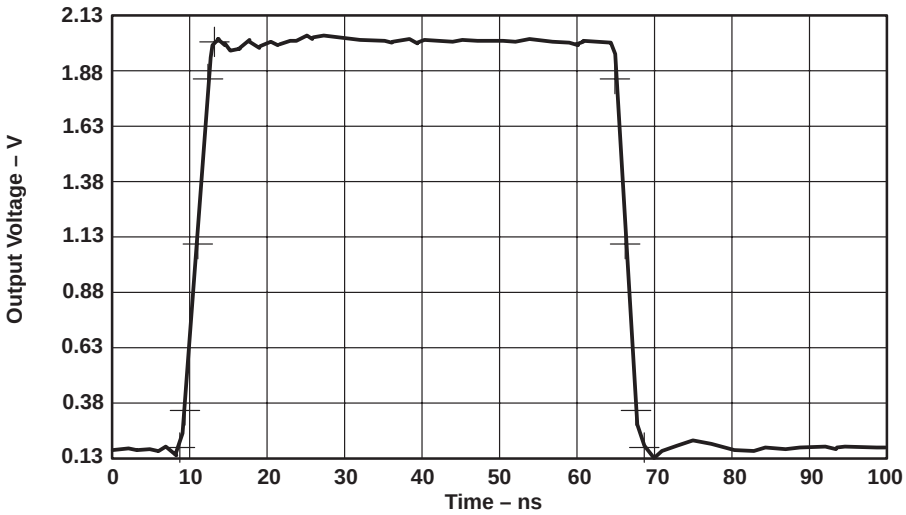
Figure 33. Observed Waveforms With a 45-Degree Bend (See Figure 31)



(a) WAVEFORMS AT TEST POINT A



(b) WAVEFORMS AT TEST POINT B



(c) WAVEFORMS AT TEST POINT C

Figure 34. Observed Waveforms With a 90-Degree Bend (See Figure 32)

Summary

In summary, the designer of high-speed systems that include AS devices must take into account the effects of the operating environment. As the system operating speed increases, the requirement for better control of the operating environment also increases. The designer of such systems must be aware not only of all the characteristics of the individual devices that are designed into the system, but also of all interactions between those devices and the source and load circuits with which they interface.

System models are very helpful in aiding the designer to understand:

- How waveforms are affected by line length.
- How (and when) to terminate signals.
- How fanout affects waveforms and can influence the choice of termination devices.

The mounting of the devices and associated effects of ground planes and conductors must also be considered.

This report has presented the basic essentials of high-speed logic design with special emphasis on the TI AS family of devices. The concepts presented are appropriate for all high-speed digital designs.

Acknowledgment

The author of this document is Mike Higgs.

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Appendix A

Confirmation of AS Model

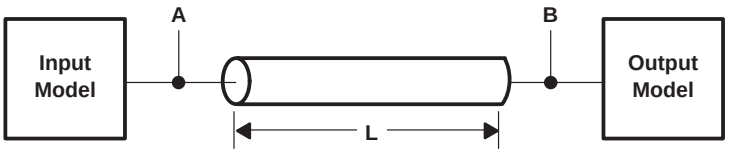

Figure 35. Observed Waveforms

Key to observed and simulated waveforms in Figure 36 for low-to-high transitions at nodes A and B shown in Figure 35:

(a) at node A for L = 4 in.
(b) at node B for L = 4 in.
(c) at node A for L = 6.5 in.
(d) at node B for L = 6.5 in.
(e) at node A for L = 9 in.
(f) at node B for L = 9 in.
(g) at node A for L = 20 in.
(h) at node B for L = 20 in.

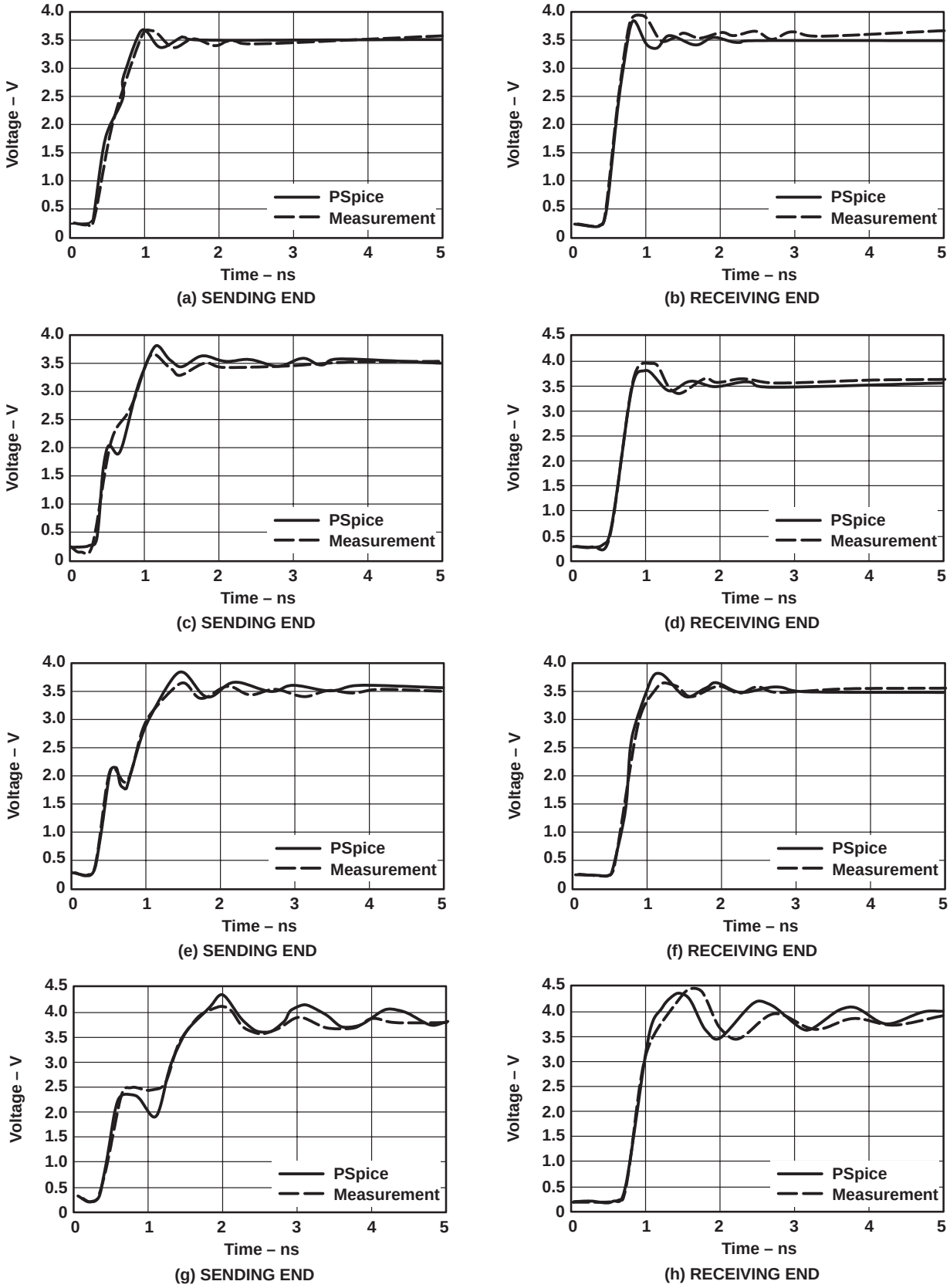

Figure 36. Comparison of Waveforms (See Figure 35)

Appendix B

Transmission Lines: A Fourier Analysis

From equation 2:

$$\frac{d^2v}{dx^2}(t,x) = L_O C_O \frac{d^2v}{dt^2}(t,x) \quad \textbf{(46)}$$

If f(x) transforms to F(s), $f'(x) \rightarrow i\,2\pi\,s\,F(s)$ by the derivative theorem. Therefore, equation 46 becomes:

$$(i\ 2\pi\ s)^2 V = L_O C_O \frac{d^2V}{dt^2} \quad \textbf{(47)}$$

Where:

$i = \sqrt{-1}$

V = voltage waveform in Fourier domain

$$-4\pi^2 s^2 V = L_O C_O \frac{d^2V}{dt^2} \quad \textbf{(48)}$$

$$\frac{d^2V}{dt^2} + \frac{4\pi^2 s^2 V}{L_O C_O} = 0 \quad \textbf{(49)}$$

Equation 49 is a second-order, linear, homogeneous equation whose solution is shown in equation 50.

$$V = C_1 \cos\frac{2\pi st}{\sqrt{L_O C_O}} + C_2 \sin\frac{2\pi st}{\sqrt{L_O C_O}} \quad \textbf{(50)}$$

Let $b = vt = \frac{t}{\sqrt{L_O C_O}}$, then V becomes:

$$V = C_1 \cos(b\ 2\pi\ s) + C_2 \sin(b\ 2\pi\ s) \quad \textbf{(51)}$$

This equation is the impulse response of the transmission-line model in the Fourier domain.

[Brac 78] asserts that:

$$\cos\ \pi s \text{ transforms to }][\,(x) \quad \textbf{(52)}$$

and:

$$\sin\ \pi s \text{ transforms to }]_[\,(x) \quad \textbf{(53)}$$

Where:

$$][\,(x) \triangleq \frac{1}{2}\left[\delta\left(x + \frac{1}{2}\right) + \delta\left(x - \frac{1}{2}\right)\right] \quad \textbf{(54)}$$

and:

$$]_[\,(x) \triangleq \frac{1}{2}\left[\delta\left(x + \frac{1}{2}\right) - \delta\left(x - \frac{1}{2}\right)\right] \quad \textbf{(55)}$$

In equations 54 and 55, $\delta(x)$ is the unit impulse or Dirac function.

Equations 52 through 55 and the following theorems are used to find the impulse response in the time domain.

Addition:

$$F(s) + G(s) \text{ transforms to } f(x) + g(x) \quad \textbf{(56)}$$

Similarly:

$$F(bs) \text{ transforms to } \frac{1}{|b|} f\left(\frac{x}{b}\right) \quad \textbf{(57)}$$

Therefore:

$$V_t(x) = \frac{C_1}{|2b|} \;] \, [\left(\frac{x}{2b}\right) + \frac{C_2 i}{|2b|} \;] \, [\left(\frac{x}{2b}\right) \quad \textbf{(58)}$$

or:

$$V_t(x) = \frac{C_1}{|4b|}\left[\delta\left(\frac{x}{2b} + \frac{1}{2}\right) + \delta\left(\frac{x}{2b} - \frac{1}{2}\right)\right] + \frac{C_2 i}{|4b|}\left[\delta\left(\frac{x}{2b} + \frac{1}{2}\right) - \delta\left(\frac{x}{2b} - \frac{1}{2}\right)\right] \quad \textbf{(59)}$$

Redefining constants and assuming $x \geq 0$:

$$V_t(x) = C_1\delta\left(\frac{x}{2b} - \frac{1}{2}\right) + C_2 i\delta\left(\frac{x}{2b} - \frac{1}{2}\right) \quad \textbf{(60)}$$

Another approach is to take advantage of the theorem of modulation [Brac 78]:

$$F(s) \cos \omega s \text{ transforms to } \frac{1}{2}\left[f\left(x - \frac{\omega}{2\pi}\right) + f\left(x + \frac{\omega}{2\pi}\right)\right] \quad \textbf{(61)}$$

and:

$$F(s) \sin \omega s \text{ transforms to } \frac{1}{2}\left[f\left(x + \frac{\omega}{2\pi}\right) - f\left(x - \frac{\omega}{2\pi}\right)\right] \quad \textbf{(62)}$$

Using equations 61 and 62, transform V (equation 51) to the following:

$$V_t(x) = C_1\left[\delta\left(x + \frac{2b}{2}\right) + \delta\left(x - \frac{2b}{2}\right)\right] + iC_2\left[\delta\left(x + \frac{2b}{2}\right) - \delta\left(x - \frac{2b}{2}\right)\right] \quad \textbf{(63)}$$

Finally, using the condition that $V_O + (0) = \delta(0) = 1$, C_1 and C_2 are unity.

Hence, the impulse response to the transmission-line model is:

$$V_t(x) = \delta(x - b) + \delta(x + b) \quad \textbf{(64)}$$

If the definition b = vt is used, equation 64 becomes:

$$V_t(x) = \delta(x - vt) + \delta(x + vt) \quad \textbf{(65)}$$

Finally, with $t \geq 0$, the transform can be qualified with the unit step, H(t), where:

$H(t) = 0, \; t < 0$
$H(t) = 1, \; t > 0$

Thus:

$$V_t(x) = \delta(x - vt) \; H(x - vt) \quad \textbf{(66)}$$

If the impulse response is called V_i, and with any input signal V_S, the voltage seen on the transmission line is V_O, the convolution of V_i and V_S is:

$$V_O = V_i * V_s \quad \textbf{(67)}$$

Convolution corresponds to multiplication in the Fourier domain.

$$f(x) * g(x) \rightarrow F(s)\ G(s) \tag{68}$$

$$V_O = V_i V_s = V_i \cos(b\ 2\pi\ s) + V_i \sin(b\ 2\pi\ s) \tag{69}$$

Again, by using the modulation theorem:

$$V_O = V_i(x - vt)\ H(x - vt) \tag{70}$$