Application Note

TAS2118/TAS2020/TAS2120/TAS2320 2-Layer PCB Design Guidelines

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ABSTRACT

Texas Instruments audio amplifiers portfolio cover a wide spectrum of audio applications, ranging from the Simple Amplifiers through IV-sense enabled Smart Amplifiers all the way to Integrated DSP with IV-sense Smart Amplifiers. Simple Amplifiers are they way to go for basic applications where cost and implementation simplicity are the most important requirements, whereas IV-sense enabled with integrated DSP amplifiers are purposed mainly for high-end devices where sound quality and more advanced tuning requirements are a higher priority.

TI's latest family of simple audio amplifiers TAS2118, TAS2020, TAS2120 and TAS2320 are available in VQFN-HR package. This package enables cheaper and simpler PCB fabrication processes, including PCB's with only two copper layers, making TI's simple amplifiers easier to implement in a wide range of applications and all that at lower fabrication costs.

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Trademarks

1 Introduction

TAS2118 and TAS2x20 family of devices offer a wide selection in speaker power range. This document uses TAS2120 as baseline for the design recommendations, however the same approach can be applied to the other variants by removing the inductor related components and layout for the TAS2020 and TAS2320 options.

For a detailed description of component selection and PCB layout design requirements for high performance systems, see TAS2x20 Design and Layout Guidelines.

For any specific questions or support in schematic and PCB layout review, post a new thread at TI E2E support forums.

2 Application Schematics

This document is focused on the 1S boosted configuration as described in Figure 2-1. A single-cell battery or similar supply in the range of 2.5V to 5.5V is used as the voltage source to power up the device.

Even though this document focuses on on 1S boosted configuration, TAS2120 also support 2S and 3S battery configurations, which can be used to achieve even higher output power range. For further details, see the TAS2120 datasheet and TAS2120EVM user's guide.

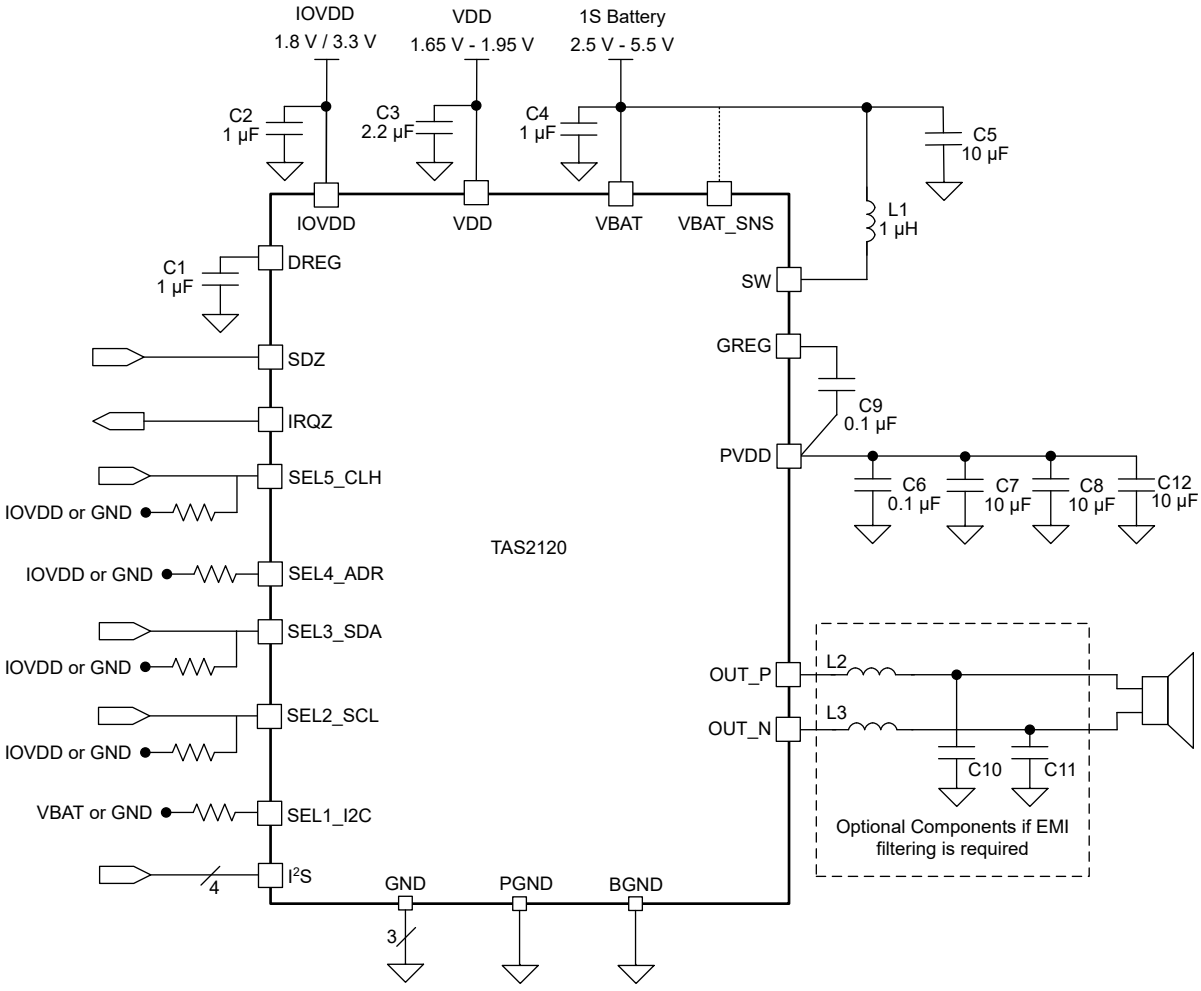

Figure 2-1. Application Diagram for 1S Boosted Configuration

2.1 Recommended Component Ratings

Table 2-1 lists the recommended component ratings for the components shown in Figure 2-1.

Table 2-1. Component Ratings

Component	Description	Specification	Min	Typical	Max	Unit
L1	Boost Converter Inductor	Inductance	0.47	1	-	µH
		Saturation Current	-	5.3	-	A
L2, L3	Optional EMI Filter Inductors	DC Current	2	-	-	A
C1, C2	DREG, IOVDD decoupling capacitors	Capacitance 20% tolerance	-	1	-	µF
		Voltage Rating	2	6.3	-	V
C3	VDD decoupling capacitor	Capacitance 20% tolerance	-	2.2	-	µF
		Voltage Rating	4	6.3	-	V
C4	VBAT decoupling capacitor	Capacitance 20% tolerance	-	1	-	µF
		Voltage Rating	6.3	10	-	V
C5	VBAT power decoupling capacitor	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	6.3	10	-	V
C5a	VBAT2S decoupling capacitor	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	10	16	-	V
C6	PVDD Low-ESL decoupling capacitor	Capacitance 20% tolerance	-	0.1	-	µF
		Voltage Rating	16	25	-	V
C7, C8, *C12	PVDD Power decoupling capacitors. C12 required only for Boost output >13V	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	16	25	-	V
		De-rated capacitance at 13V of the combined PVDD capacitor	3	-	-	µF
C9	GREG decoupling capacitor	Capacitance 20% tolerance	-	0.1	-	µF
		Voltage Rating	6.3	10	-	V
C10, C11	Optional EMI Filter capacitors (must use L2, L3 if C10, C11 are used)	Voltage Rating	2xPVDD		-	V

Function selection pins in hardware mode must be connected to IOVDD, VBAT or GND using specific resistor values for each of the options, follow the Table 2-2 table to select the correct component values.

Table 2-2. Hardware Select Pin Resistor Values

Hardware Select Pin	Resistor Value	Description
SEL1	0Ω to VBAT	21dBV and Volume Ramp Enabled
	24kΩ to VBAT	18dBV and Volume Ramp Enabled
	24kΩ to GND	12dBV and Volume Ramp Enabled
	5kΩ to VBAT	6dBV and Volume Ramp Enabled
	330Ω to VBAT	21dBV and Volume Ramp Disabled
	5kΩ to GND	18dBV and Volume Ramp Disabled
	1.2kΩ to VBAT	12dBV and Volume Ramp Disabled
	1.2kΩ to GND	6dBV and Volume Ramp Disabled
	0Ω to GND	I^2C Mode
SEL2	1.2kΩ to IOVDD	Left Justified Right Channel or TDM Slot 4
	5kΩ to GND	Left Justified Mix or TDM Slot 5
	5kΩ to IOVDD	TDM Slot 6
	24kΩ to GND	TDM Slot 7
	1.2kΩ to GND	Left Justified Left Channel or TDM Slot 3
	0Ω to IOVDD	I^2S Mix or TDM Slot 2
	330Ω to IOVDD	I^2S Right Channel or TDM Slot 1
	0Ω to GND	I^2S Left Channel or TDM Slot 0
SEL3	0Ω to IOVDD	Rising edge of SBCLK
	0Ω to GND	Falling edge of SBCLK
SEL4	24kΩ to IOVDD	Address 0x94 or Y-Bridge Threshold 1mW
	0Ω to IOVDD	Address 0x96 or Y-Bridge Threshold 40mW
	24kΩ to GND	Address 0x92
	0Ω to GND	Address 0x90 or Y-Bridge Threshold 80mW
SEL5	0Ω to GND	TAS2120: VBAT 1S Mode TAS2320: N/A
	24kΩ to IOVDD	TAS2120: VBAT 2S Mode TAS2320: N/A
	0Ω to IOVDD	TAS2120: External PVDD mode (2.5V to 14V) TAS2320: External PVDD mode (2.5V to 14V)

3 Design Guidelines

3.1 Hardware Control Reference Schematic

TAS2120 2-Layer HW Control Reference Schematic – DUT Section shows the schematic used in the TAS2120 2-Layer Evaluation Module for a hardware control configuration, which is used to design the PCB described in the later section.

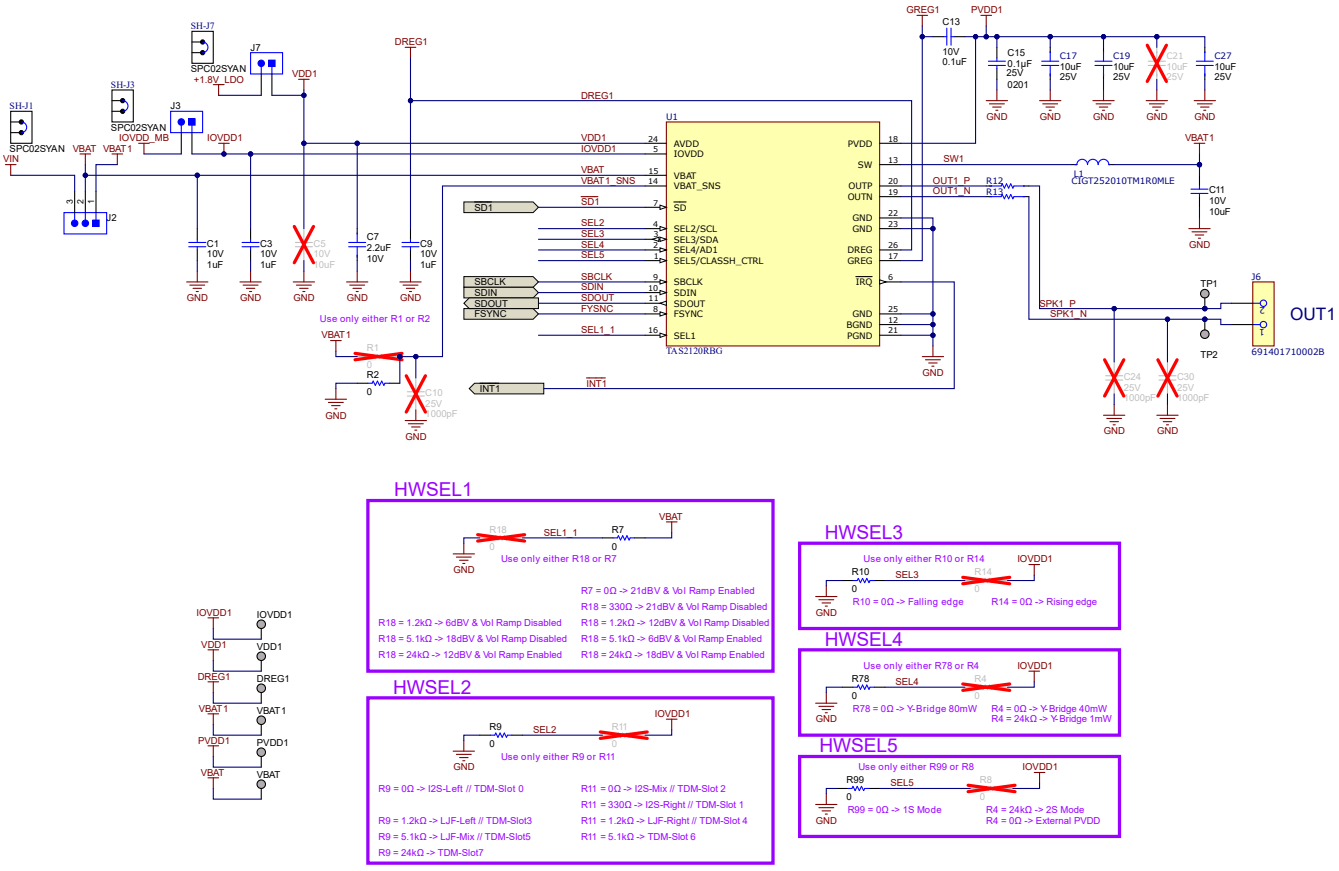

Figure 3-1. TAS2120 2-Layer HW Control Reference Schematic – DUT Section

3.2 Hardware Control Reference PCB Layout

Most of the signals and power traces are laid out on the same layer as the IC. Consider all the critical components to be placed close to the IC and the routing similar to the described in TAS2x20 Design and Layout Guidelines Section 3. The following sections provide further guidance on each of the critical signals. TAS2120 is considered a superset of the rest of the variants, so a similar approach can be used as baseline, making the necessary adjustments given the pin function differences.

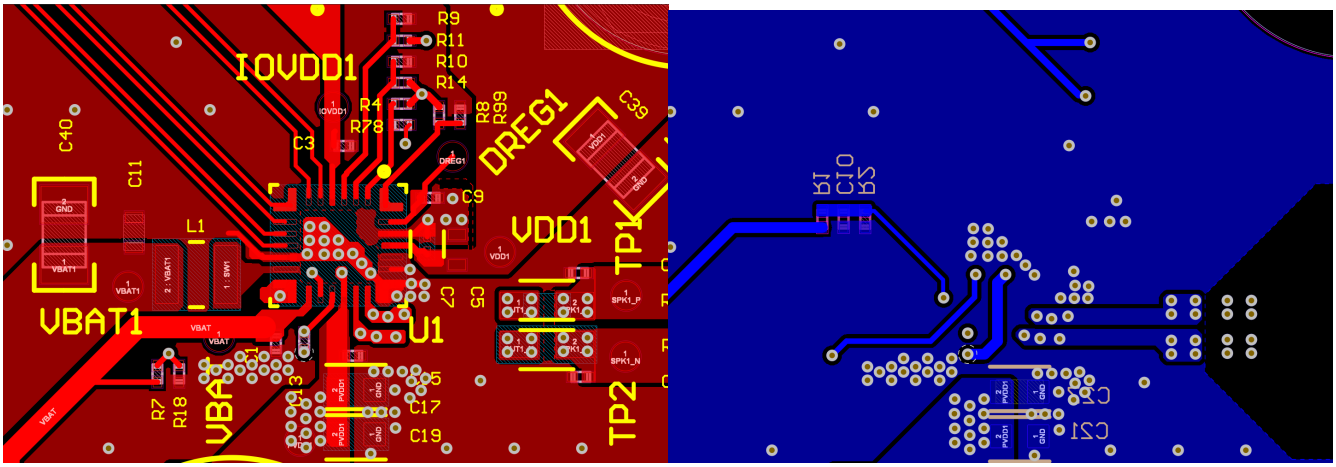

Figure 3-2. Top (Red) and Bottom (Blue) Layer – Hardware Control Reference PCB Layout

3.2.1 GND Connections

- The top layer is poured with GND at all places that no other signal is required.
- It is encouraged to add via stitching to the GND planes from top to bottom layers for better thermal and electrical performance.
- Make sure GND pin 25 is not directly connected to PGND and BGND pins 21 and 12, use vias instead to connect to GND on the bottom layer.
- Add several vias to GND under the IC and make sure there is a direct connection between PGND and BGND pins 21 and 12 on top layer itself.
- Add several vias to GND close to the decoupling capacitors for VBAT and PVDD pins, as well as close to PGND pin 21.

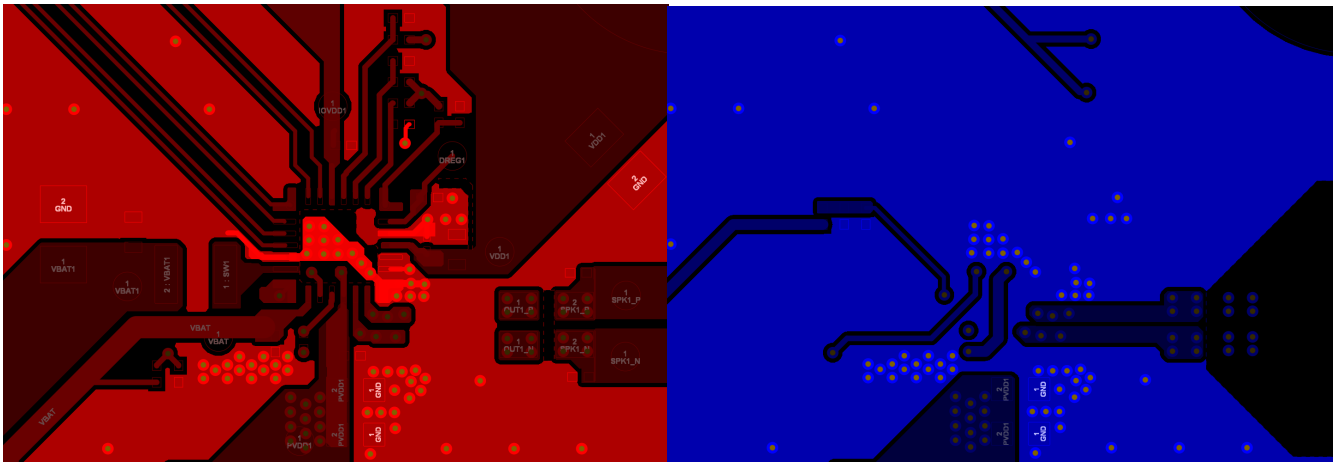

Figure 3-3. Top (Red) and Bottom (Blue) Layer – GND Connections HW Control

3.2.2 Power Connections

- Place the decoupling capacitors close to each of the power pins VBAT, PVDD, IOVDD, VDD and DREG.
- Place the SW inductor as close to the IC as possible, add the bulky VBAT decoupling capacitors close to SW inductor.
- If using PVDD decoupling capacitors on both top and bottom layers, add several vias to connect these together.

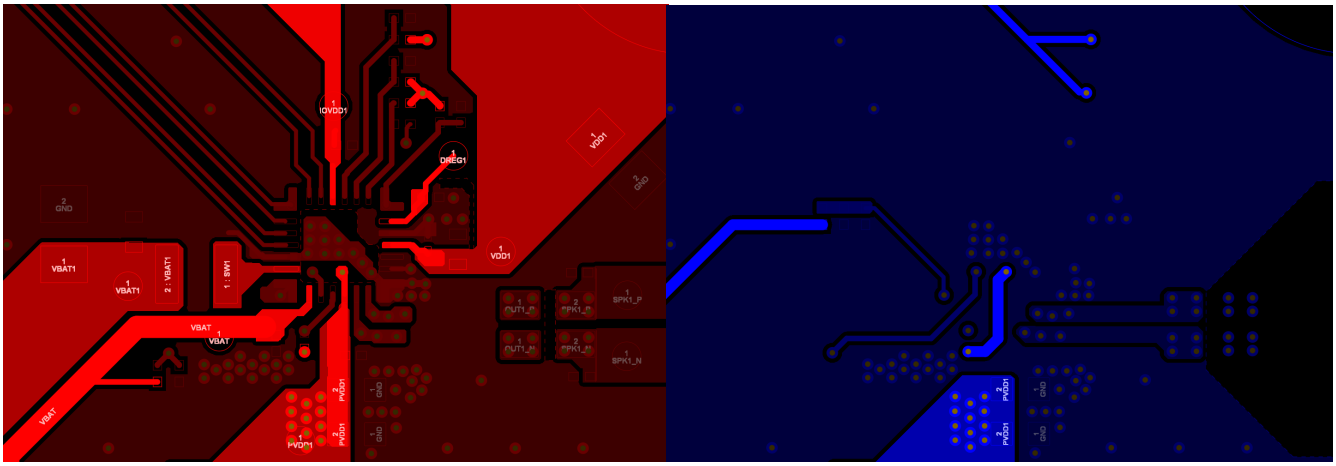

Figure 3-4. Top (Red) and Bottom (Blue) Layer – Power Connections HW Control

3.2.3 Output Connections

- Fanout the output traces on the opposite side of the PCB, in this case the bottom layer, such that PGND pin 21 is directly connected to the decoupling capacitors on PVDD without layer changes.
- Use at least three vias to change from top to bottom layer for each of the output traces.
- Route the output traces differentially and keeping the resulting impedance as close to each other as possible.

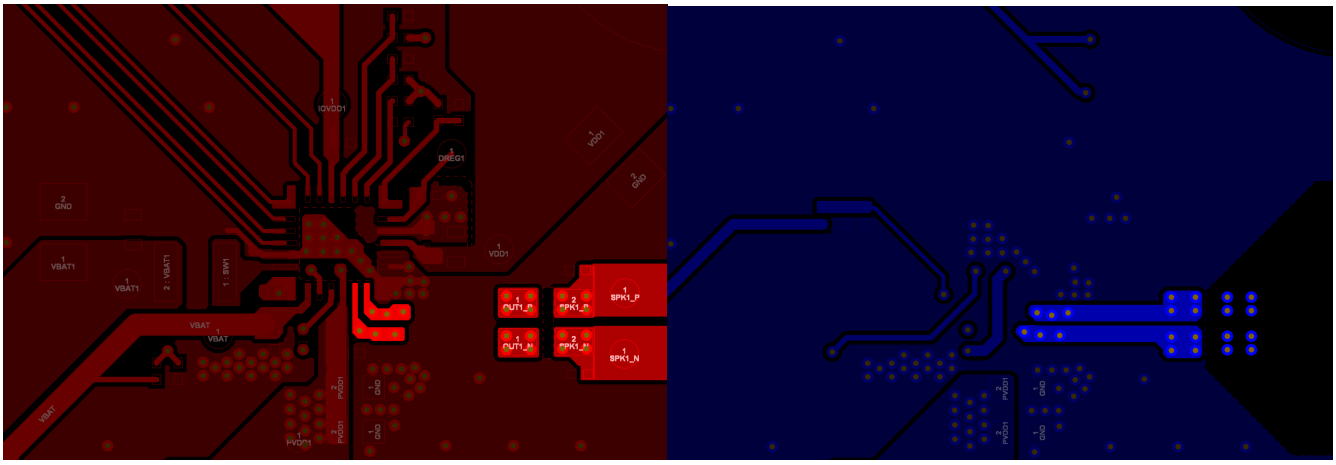

Figure 3-5. Top (Red) and Bottom (Blue) Layer – Output Connections HW Control

3.2.4 GREG Connection

- Place a via for PVDD under the IC to connect the GREG capacitor. This allows a star connection away from the PVDD decoupling capacitors.

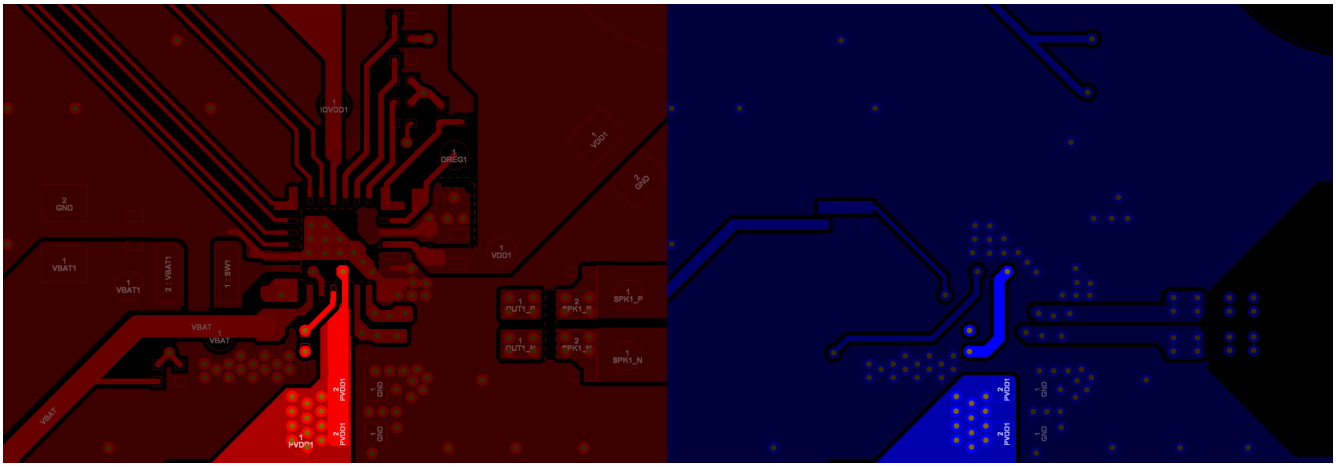

Figure 3-6. Top (Red) and Bottom (Blue) Layer – GREG Connection HW Control

3.2.5 Input and SEL Connections

- Fanout the digital audio signals on a single layer such that the opposite layer is as solid GND pour as possible.
- In this example each of the SEL pins connect to 0Ω stuff options to select the different options. On a final product these connections can be simplified connecting to nearby IOVDD or GND traces.
- During layout, treat SEL connections with lower priority compared to Power and GREG connections.

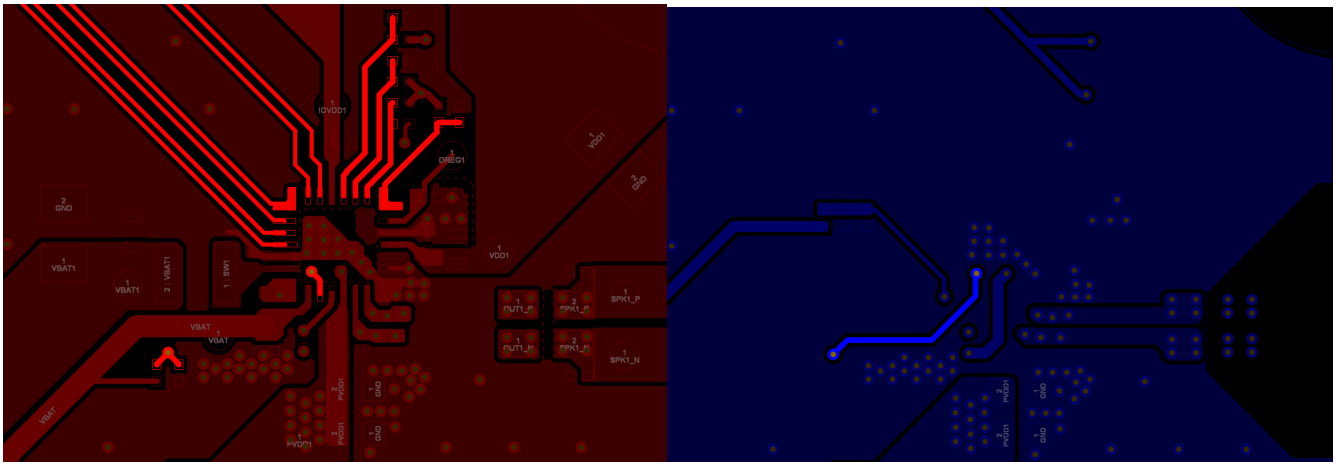

Figure 3-7. Top (Red) and Bottom (Blue) Layer – Input and SEL Connections

3.3 Software Control Reference Schematic

TAS2120 2-Layer SW Control Reference Schematic – DUT Section show the schematic used in TAS2120 2-Layer Evaluation Module for a software control configuration.

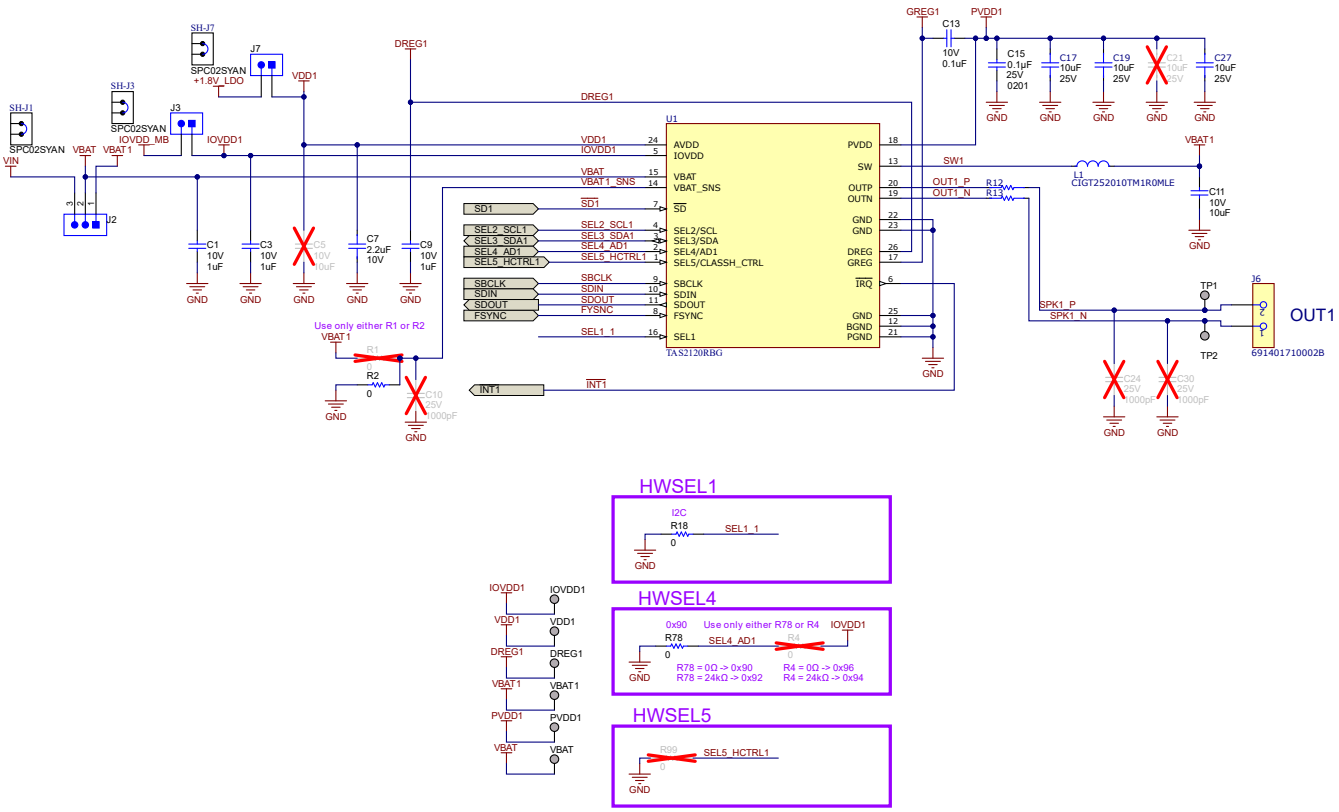

Figure 3-8. TAS2120 2-Layer SW Control Reference Schematic – DUT Section

3.4 Software Control Reference PCB Layout

The following figures show a similar implementation as Section 3.2 but for I²C mode. All GND, GREG, Power and Output connections are the same, just changing the SEL pins for I²C control instead.

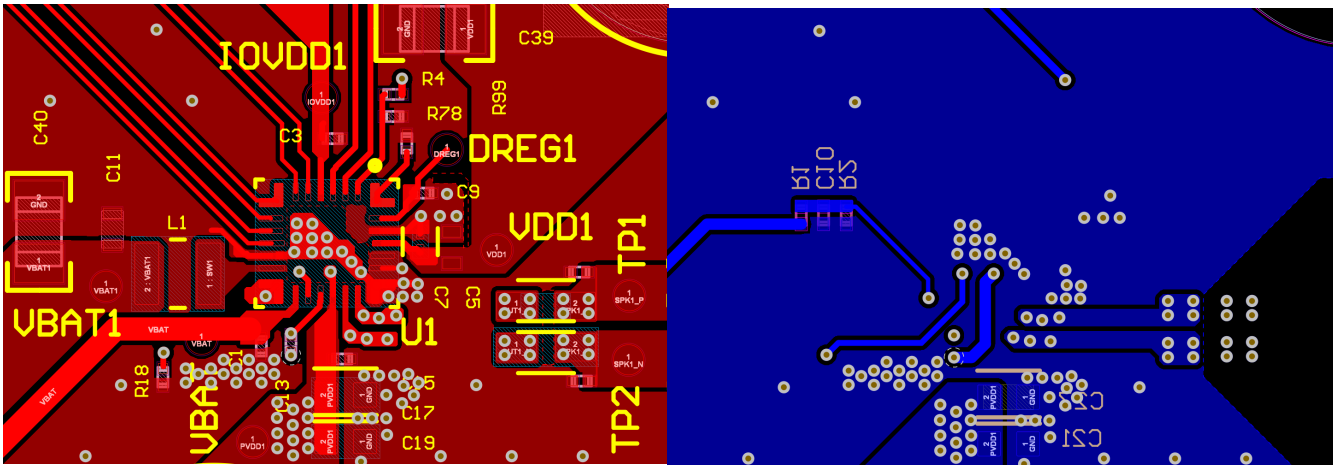

Figure 3-9. Top (Red) and Bottom (Blue) Layer – Software Control Reference PCB Layout

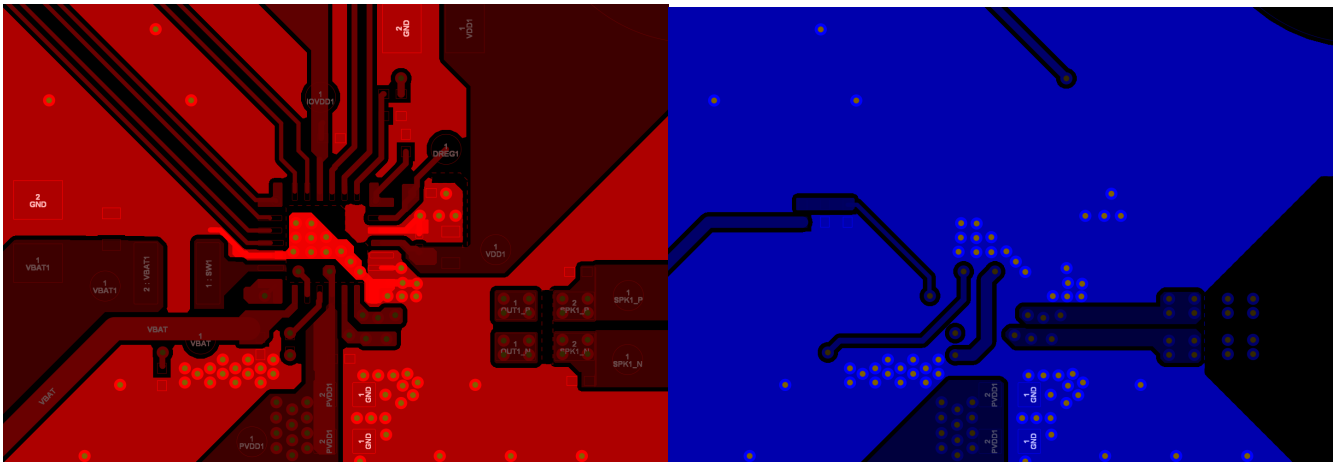

Figure 3-10. Top (Red) and Bottom (Blue) Layer – GND Connections SW Control

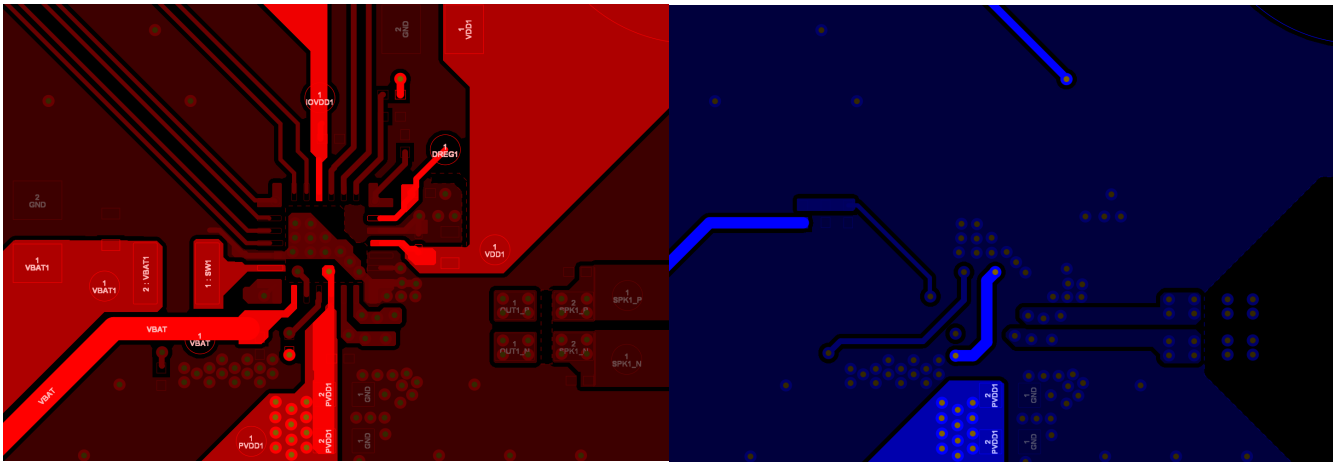

Figure 3-11. Top (Red) and Bottom (Blue) Layer – Power Connections SW Control

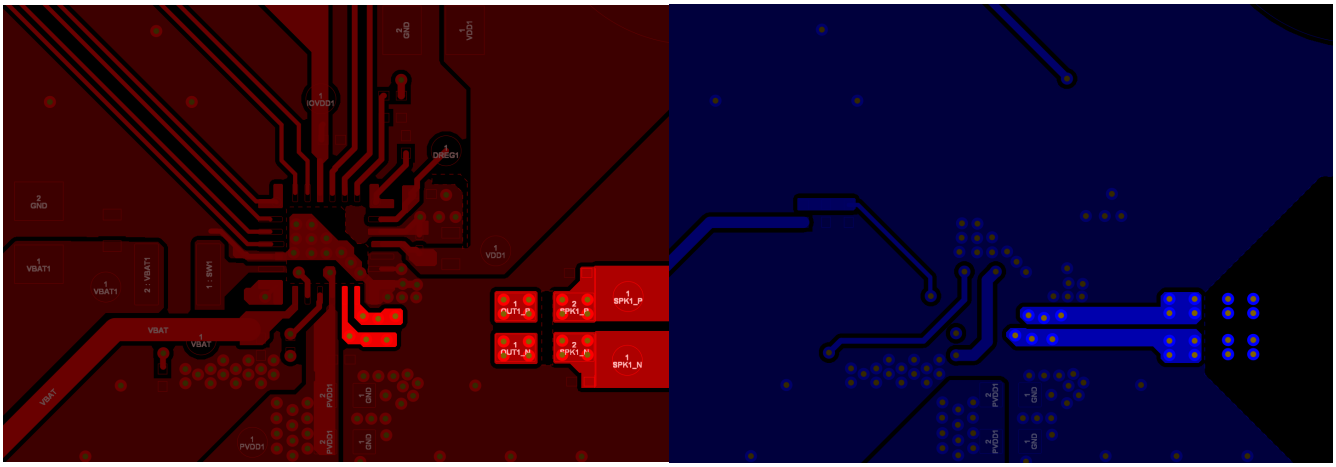

Figure 3-12. Top (Red) and Bottom (Blue) Layer – Output Connections SW Control

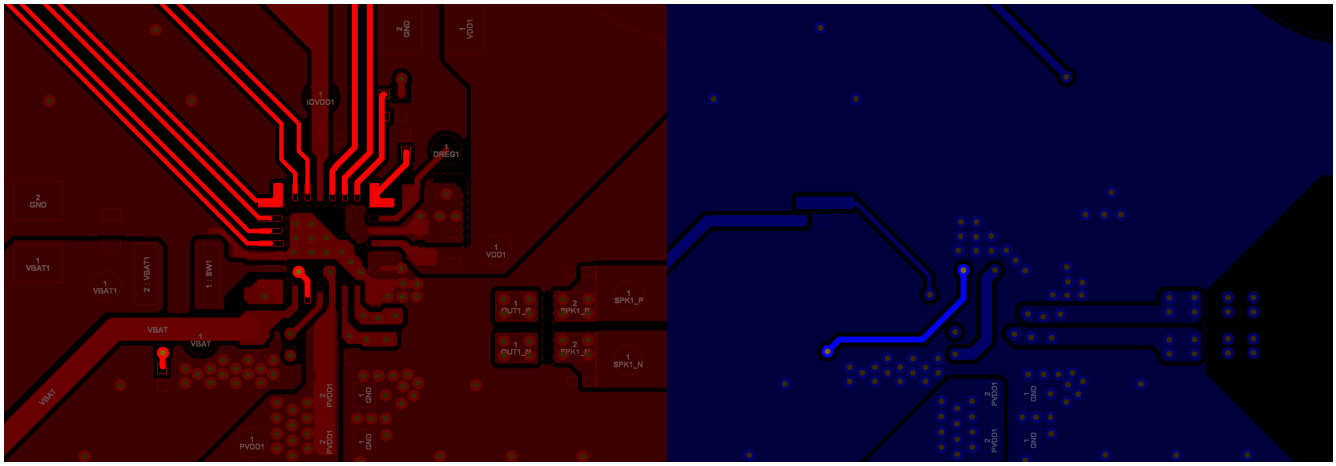

Figure 3-13. Top (Red) and Bottom (Blue) Layer – GREG Connection SW Control

4 Summary

This application note provides comprehensive 2-layer PCB design guidelines for Texas Instruments' family of simple audio amplifiers, specifically the TAS2118, TAS2020, TAS2120, and TAS2320.

These devices are housed in VQFN-HR packages, which are designed to support cost-effective and simple PCB fabrication processes using only two copper layers.

The document focuses on the 1S boosted configuration, utilizing a single-cell battery supply ranging from 2.5V to 5.5V, though it notes that the TAS2120 also supports 2S and 3S battery configurations for higher power output.

Key technical content includes:

- Application Schematics: Detailed diagrams for both hardware-controlled and software-controlled (I^2C) configurations.
- Component Ratings: Recommended specifications for critical components, including boost converter inductor, decoupling capacitors (DREG, IOVDD, VDD, PVDD, VBAT, and GREG), and optional EMI filter components.
- Hardware Configuration: A reference table for selecting device functions (such as volume ramp and dBV levels) via specific resistor values on the SEL pins.
- PCB Layout Best Practices: Specific design guidance to verify electrical and thermal performance, covering:
  - GND Connections: Strategies for via stitching, GND plane pours, and proper separation of PGND and BGND pins.
  - Power Input & Output: Placement of decoupling capacitors close to pins, inductor proximity to the IC, and differential routing for output traces.
  - Signal Integrity: Guidelines for GREG connections, digital audio signal fanout, and SEL pin layout priority.

5 References

1. Texas Instruments, *TAS2x20 Design and Layout Guidelines*, application note.
2. Texas Instruments, *TAS2120 Evaluation Module User's Guide*, user's guide.
3. Texas Instruments, *TAS2320 Evaluation Module User's Guide*, user's guide.
4. Texas Instruments, *TAS2020 Evaluation Module User's Guide*, user's guide.
5. Texas Instruments, *TAS2118 Evaluation Module User's Guide*, user's guide.

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