Application Note

FAQs on UCC25661x

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ABSTRACT

This application note discusses the most frequently asked questions of the UCC25661x LLC resonant controller when used in different applications.

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1 UCC25661x Frequently Asked Questions

1.1 How to Connect External Gate Drivers to the UCC25661x for High Gate Driver Current Capability?

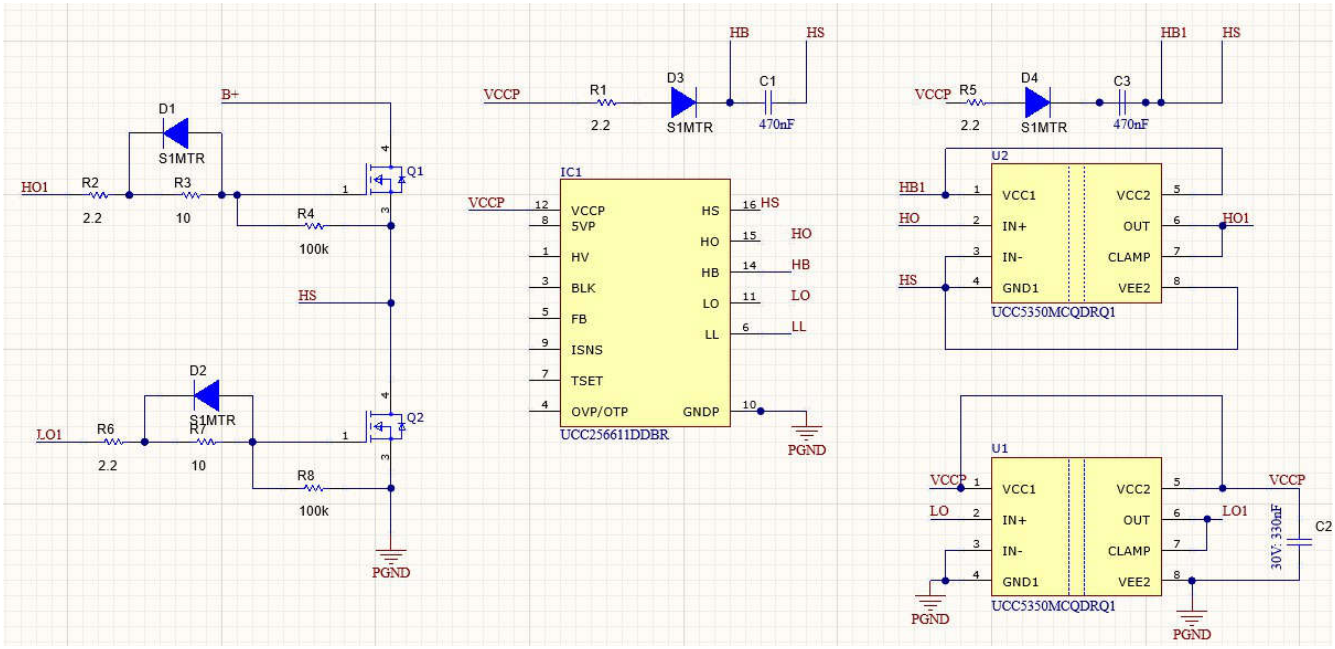

Figure 1-1. External Driver Interface with UCC25661x

Figure 1-1 shows a simpler way of connecting external gate drivers to the UCC25661x. Here two drivers such as UCC5350MCQDRQ1 are used which has a higher output current capability. Here the external high side driver is bootstrapped just like the internal driver of the UCC25661x.

1.2 Up To What Switching Frequency Controller Can Operate?

UCC25661x family can operate up to a 750kHz switching frequency.

1.3 While Operating UCC25661x, 1 Second Fault is Coming. How to Debug it?

If the controller is giving LO pulses and then there is no pulse from the controller side and the controller is retrying after 1 sec, this is due to either the OCP fault or OLP fault. For OCP fault detection, the voltage across the ISNS pin and PGND has to be probed. If the peak voltage at the ISNS pin touches the threshold of 3.5V, it is the OCP fault. To avoid OCP fault, R_{isns} must be reduced gradually, and TSET resistor divider must be adjusted accordingly by the design calculator to accommodate P_{in} vs VFBReplica graph within 2V-4V for no load to full load variation.

For OLP fault detection, FBReplica vs Pin graph has to be fitted one first prototype. The procedure to measure FBReplica in practical hardware is as follows:

1. Measure FBReplica voltage by inserting 5k resistor between feedback optocoupler emitter and ground as shown in Figure 1-2. The calculation can be done by Equation 1 .

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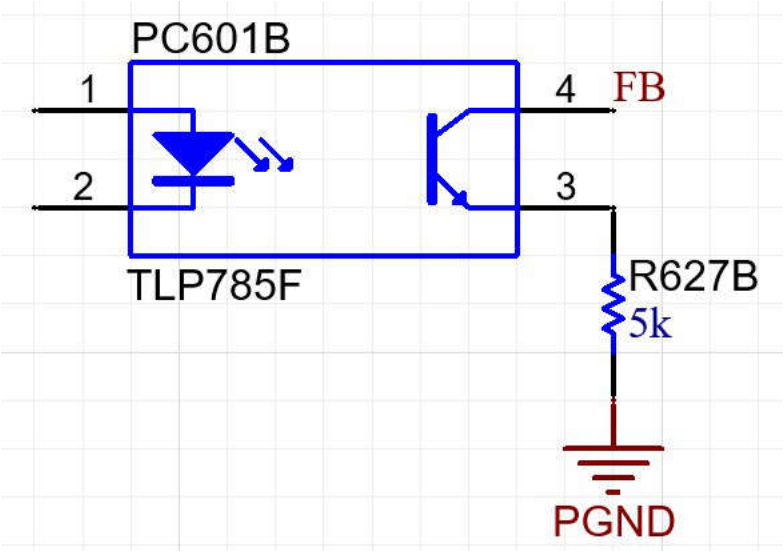

Figure 1-2. FBReplica Measurement Circuit

$$FBReplica = \left(I_{FB} - \frac{V_{5k}}{5k}\right) \times R_{FBInternal} \# (1) \quad (1)$$

2. Plot FBReplica voltage vs Pin graph at different input power up to considering peak output power, not just up to full load output power, as shown in Figure 1-3.

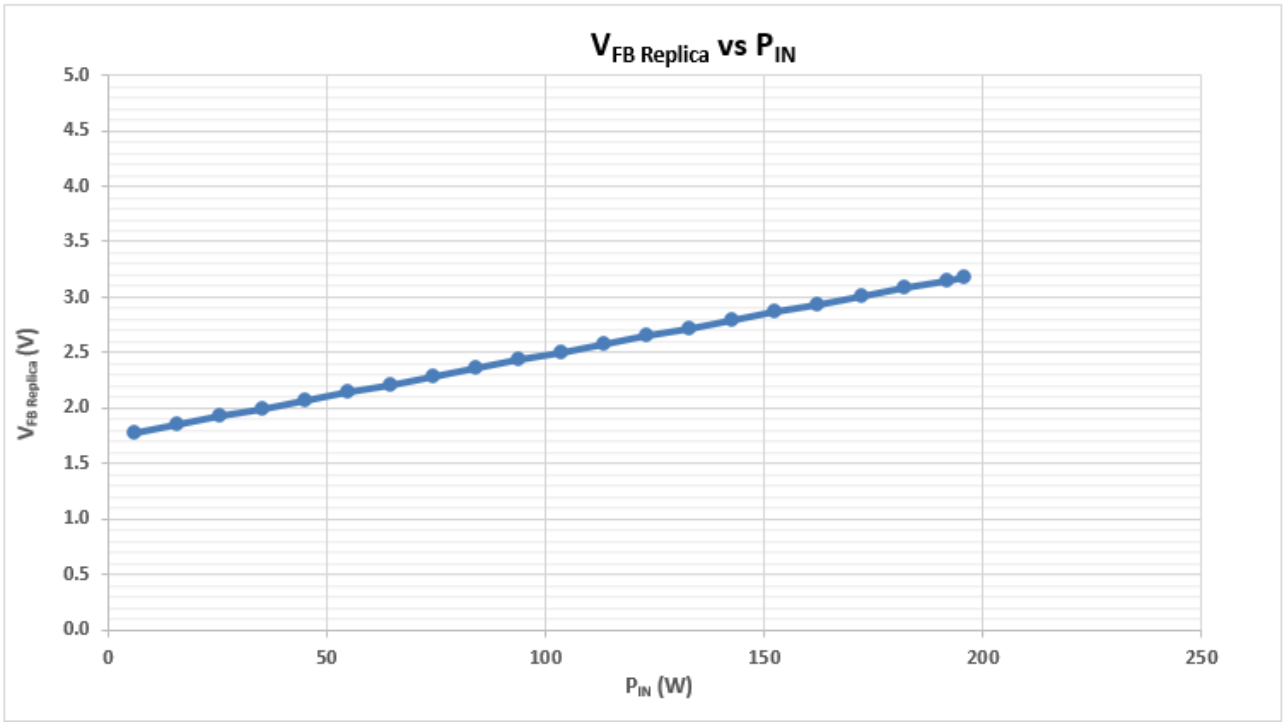

Figure 1-3. VFBReplica vs Pin Graph

If at any load, FBReplica touches 4.75V, then the fault at that load is OLP.

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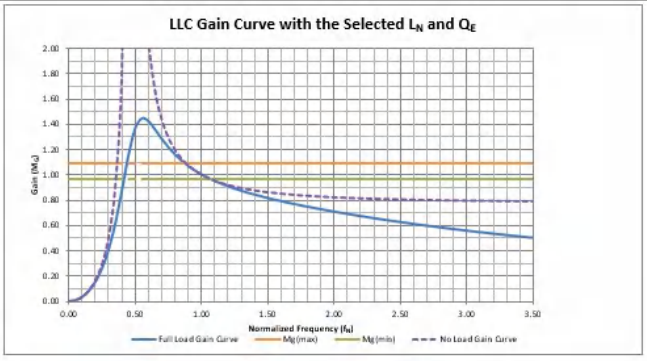
1.4 How to Implement A Battery Charger with UCC25661x?

The battery chargers exhibit different effective output resistance variation with the change in output voltages. In case of battery chargers, the effective output resistance increases with the output voltage whereas in case of LED drivers, the voltage can be reduced. When LLC is designed in these applications, we need to make sure required voltage gains are met.

The LLC tank parameters and the turns ratio are chosen based on the Vin_typ = 390V (350V-410V) , Vout_typ = 58.7V(Vout_min 46.2V- Vout_max 71.2V),

Battery charging current = 7A , f_{res} = 100kHz . Three Excel calculators must be made with typical, maximum, and minimum Vout with the same tank circuit. Make sure that Mg(min), Mg(max) lines meet with the LLC gain curve with a good margin (peak gain of LLC gain curve is at least 10-15% higher than Mg(max) at Vout_Max. The minimum gain goes below 90% of Mg(min)) as shown in Figure 1-4, Figure 1-5, and Figure 1-6

Select Which Device You Are Using		UCC256614		Refer datasheet for the difference of UCC25660x devices
OUTPUT				
Output Voltage	V_{OUT}	58.7	V	Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	410.9	W	Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	7	A	
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	120	mV	Enter the desired maximum output voltage ripple
Target Efficiency	η	0.97		Enter the Overall Efficiency here
INPUT				
Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V	Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(lo)}$	365	V	Enter the minimum input voltage
LLC STAGE				
Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
LLC Transformer				
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	3.32197615		
Actual Primary/Secondary Turns Ratio	N_{PS}	3.33		Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00		
Actual Primary/Bias Turns Ratio	N_{PB}	11.00		Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	68.5 Ω		
LLC Effective Load Resistance at Full Load	$R_{E(full\ load)}$	75.4 Ω		
LLC Gain Range				
Minimum LLC Gain	$M_{G(min)}$	**0.962**		
Maximum LLC Gain Including Losses	$M_{G(max)}$	**1.087**		
Predicted Voltage Drop Due to Losses	V_{LOSS}	0.400	V	Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E				
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Q_E point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.				
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Q_E = 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)}$ > $M_{G(max)}$				
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.45		
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.48		
Gain Required at No-Load	$M_{G(selected)}$	0.775		
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50		
The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.				



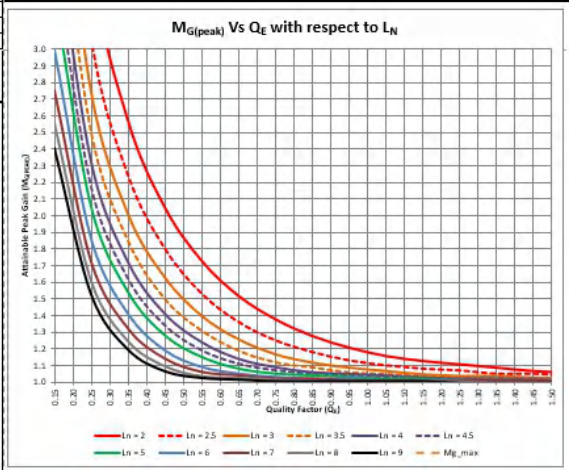


Figure 1-4. Design Calculator for Nominal Output Voltage

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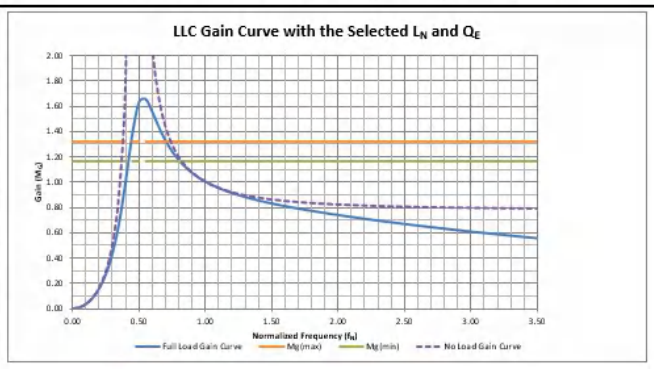
22	**Select Which Device You Are Using**		UCC256614		Refer datasheet for the difference of UCC25660x devices
23					
24	**OUTPUT**				
25	Output Voltage	V_{OUT}	71.2	V	Enter required nominal output voltage of converter
26	Maximum Output Power	P_{OUT}	498.4	W	Enter required maximum converter output power in Watts
27	Full Load Output Current	I_{OUT}	7	A	
28	Maximum Output Voltage Ripple	$V_{OUT[pk-pk]}$	120	mV	Enter the desired maximum output voltage ripple
29	Target Efficiency	η	0.97		Enter the Overall Efficiency here
30					
31	**INPUT**				
32	Nominal Input Voltage	V_{BLK}	390	V	Enter the nominal input voltage
33	Maximum DC Input Voltage	$V_{BLK[max]}$	410	V	Enter the maximum input voltage
34	Minimum DC Input Voltage	$V_{BLK[lo]}$	365	V	Enter the minimum input voltage
35					
36	**LLC STAGE**				
37	Nominal LLC Switching Frequency	f_{LLC}	100	kHz	Enter desired nominal LLC switching frequency
38	**LLC Transformer**				
39	Recommended Primary/Secondary Turns Ratio	$N_{PS[recommended]}$	2.738764045		
40	Actual Primary/Secondary Turns Ratio	N_{PS}	3.33		Enter Actual Primary/Secondary Turns Ratio
41	Recommended Primary/Bias Turns Ratio	$N_{PB[recommended]}$	13.00		
42	Actual Primary/Bias Turns Ratio	N_{PB}	11.00		Enter Actual Primary/Bias Turns Ratio
43	LLC Effective Load Resistance at 110% Full Load	R_E	83.1	Ω	
44	LLC Effective Load Resistance at Full Load	$R_{E[full load]}$	91.4	Ω	
45	**LLC Gain Range**				
46	Minimum LLC Gain	$M_{G[min]}$	**1.165**		
47	Maximum LLC Gain Including Losses	$M_{G[max]}$	**1.316**		
48	Predicted Voltage Drop Due to Losses	V_{LOSS}	0.400	V	Enter the predicted voltage drop due to conversion losses in circuit
49	**Select L_N and Q_E**				
50	**From the figure on the right, $M_{G[peak]}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Q_E point that corresponds to an Attainable $M_{G[PEAK]}$ value that is greater than $M_{G[max]}$. Enter the selected values in the L_N and Q_E cells below.**				
51					
52	For example, if $M_{G[max]}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Q_E = 0.35 would result				
53	in an attainable $M_{G[PEAK]}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G[PEAK]} > M_{G[max]}$				
54					
55	Selected Primary Inductance Ratio	$L_{N[selected]}$	3.45		
56	Selected Quality Factor for Resonant Network	$Q_{E[selected]}$	0.40		
57	Gain Required at No-Load	$M_{G[selected]}$	0.775		
58	f_N at Maximum Switching Frequency	$f_{N[max]}$	3.50		
59					
60	The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G[min]}$ and $M_{G[max]}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.				
61					



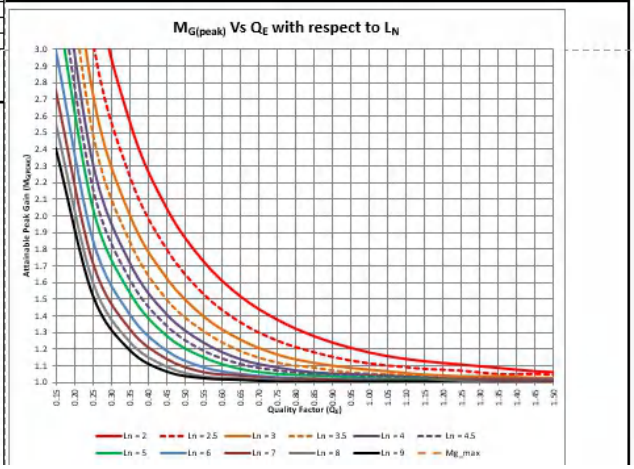


Figure 1-5. Design Calculator at Maximum Output Voltage

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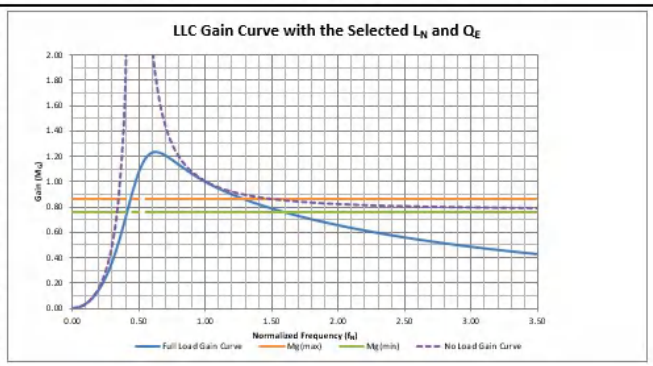
Select Which Device You Are Using		UCC256614			Refer datasheet for the difference of UCC25660x devices
OUTPUT					
Output Voltage	V_{OUT}	46.2	V		Enter required nominal output voltage of converter
Maximum Output Power	P_{OUT}	323.4	W		Enter required maximum converter output power in Watts
Full Load Output Current	I_{OUT}	7	A		
Maximum Output Voltage Ripple	$V_{OUT(pk-pk)}$	120	mV		Enter the desired maximum output voltage ripple
Target Efficiency	η	0.97			Enter the Overall Efficiency here
INPUT					
Nominal Input Voltage	V_{BLK}	390	V		Enter the nominal input voltage
Maximum DC Input Voltage	$V_{BLK(max)}$	410	V		Enter the maximum input voltage
Minimum DC Input Voltage	$V_{BLK(lo)}$	365	V		Enter the minimum input voltage
LLC STAGE					
Nominal LLC Switching Frequency	f_{LLC}	100	kHz		Enter desired nominal LLC switching frequency
LLC Transformer					
Recommended Primary/Secondary Turns Ratio	$N_{PS(recommended)}$	4.220779221			
Actual Primary/Secondary Turns Ratio	N_{PS}	3.33			Enter Actual Primary/Secondary Turns Ratio
Recommended Primary/Bias Turns Ratio	$N_{PB(recommended)}$	13.00			
Actual Primary/Bias Turns Ratio	N_{PB}	11.00			Enter Actual Primary/Bias Turns Ratio
LLC Effective Load Resistance at 110% Full Load	R_E	53.3	Ω		
LLC Effective Load Resistance at Full Load	$R_{E(full\ load)}$	53.3	Ω		
LLC Gain Range					
Minimum LLC Gain	$M_{G(min)}$	**0.759**			
Maximum LLC Gain Including Losses	$M_{G(max)}$	**0.859**			
Predicted Voltage Drop Due to Losses	V_{LOSS}	0.400	V		Enter the predicted voltage drop due to conversion losses in circuit
Select L_N and Q_E					
From the figure on the right, $M_{G(peak)}$ Vs Q_E with respect to L_N, select a point on an Ln curve that has an Ln and Q_E point that corresponds to an Attainable $M_{G(PEAK)}$ value that is greater than $M_{G(max)}$. Enter the selected values in the L_N and Q_E cells below.					
For example, if $M_{G(max)}$, calculated above and shown by the horizontal line, was calculated to be 1.4, then using Ln = 5 and Q_E = 0.35 would result in an attainable $M_{G(PEAK)}$ = 1.52 (interpolated from Ln = 5 curve) which satisfies the requirement that the Attainable $M_{G(PEAK)} > M_{G(max)}$					
Selected Primary Inductance Ratio	$L_{N(selected)}$	3.45			
Selected Quality Factor for Resonant Network	$Q_{E(selected)}$	0.61			
Gain Required at No-Load	$M_{G(selected)}$	0.775			
f_N at Maximum Switching Frequency	$f_{N(max)}$	3.50			

The selected L_N and Q_E values should result in an LLC Gain Curve, shown below, that intersects with the $M_{G(min)}$ and $M_{G(max)}$ traces. The Gain curve from an overload condition is also plotted, showing the minimum gain at maximum frequency.



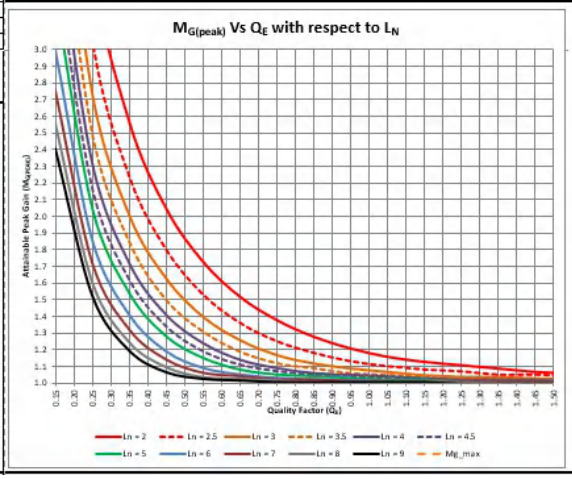


Figure 1-6. Design Calculator at Minimum Output Voltage

Battery chargers must operate in either constant current mode (CC) or constant voltage (CV), depending on the charging status of the battery and effective load resistance. Effective load resistance determines the operating point of the CC-CV controlled power supply.

Figure 1-7 shows an example of how CC-CV loop is implemented.

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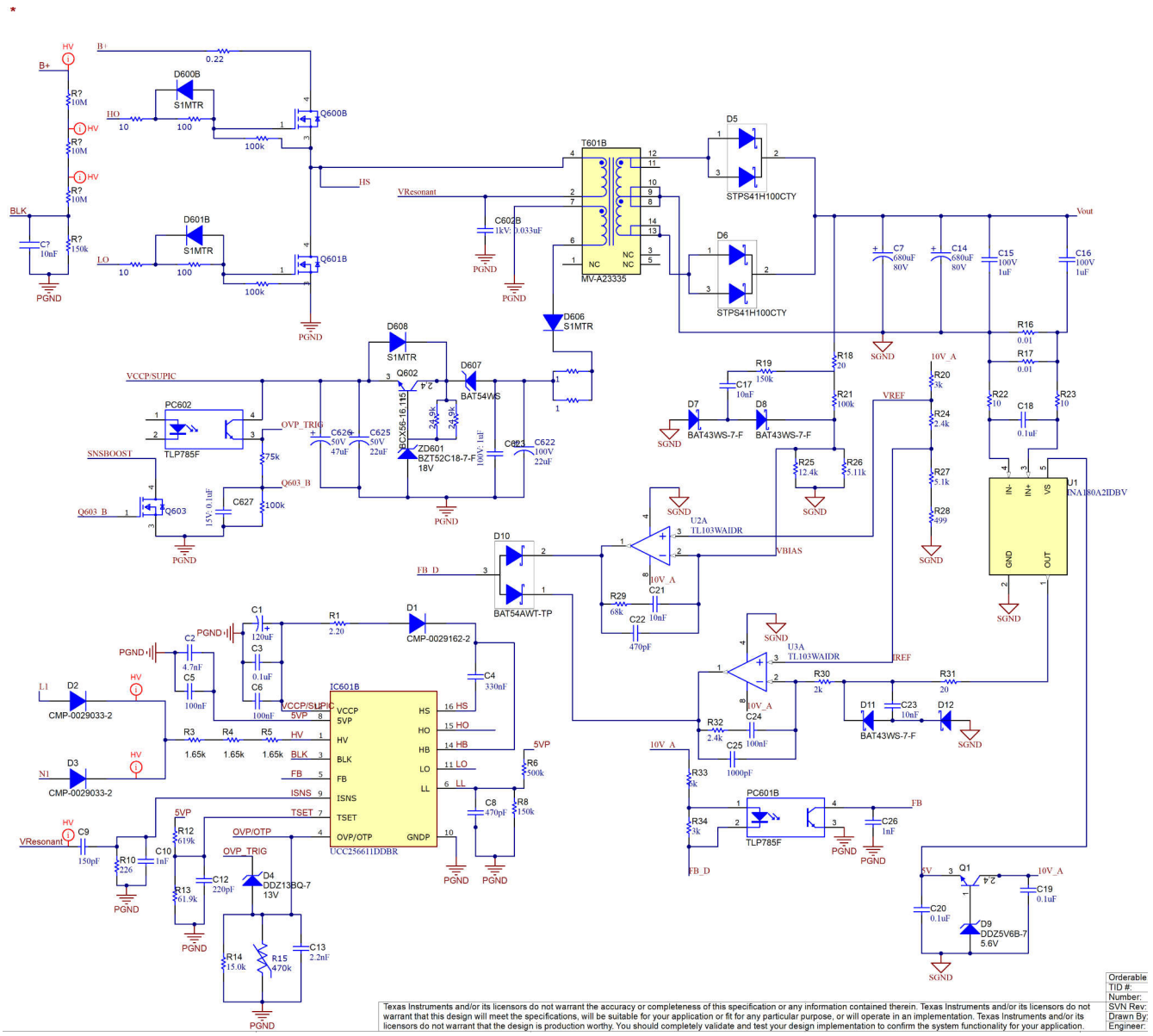

Figure 1-7. CC-CV Control Loop Circuit With UCC25661x

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1.5 How to Set Up OVP/OTP Pin?

UCC25661x family uses a multi-function pin (OVP/OTP) that monitors for output overvoltage and external over-temperature conditions. To operate the controller in normal condition, the OVP/OTP pin voltage should be in between $VOVP_{Pos}$ and $VOTP_{Neg}$. Normally, The OVP/OTP pin voltage is IOTP * NTC resistance. If Temperature is very high, NTC resistance becomes very less. Thus, OVP/OTP pin voltage becomes less than $VOTP_{Neg}$, IC will give OTP Fault.

If the output voltage of the LLC converter becomes high enough that VCCP becomes high and Zener diode in OVP/OTP pin starts conducting, then total current through NTC resistors become (Zener diode current + I_{OTP}). Therefore, the voltage at the OVP/OTP pin starts rising. If the voltage is over $VOVP_{Pos}$, IC gives OVP fault.

While designing a circuit using $VOVP_{Pos}$ and $VOTP_{Neg}$, the OVP and OTP comparator hysteresis values must be considered.

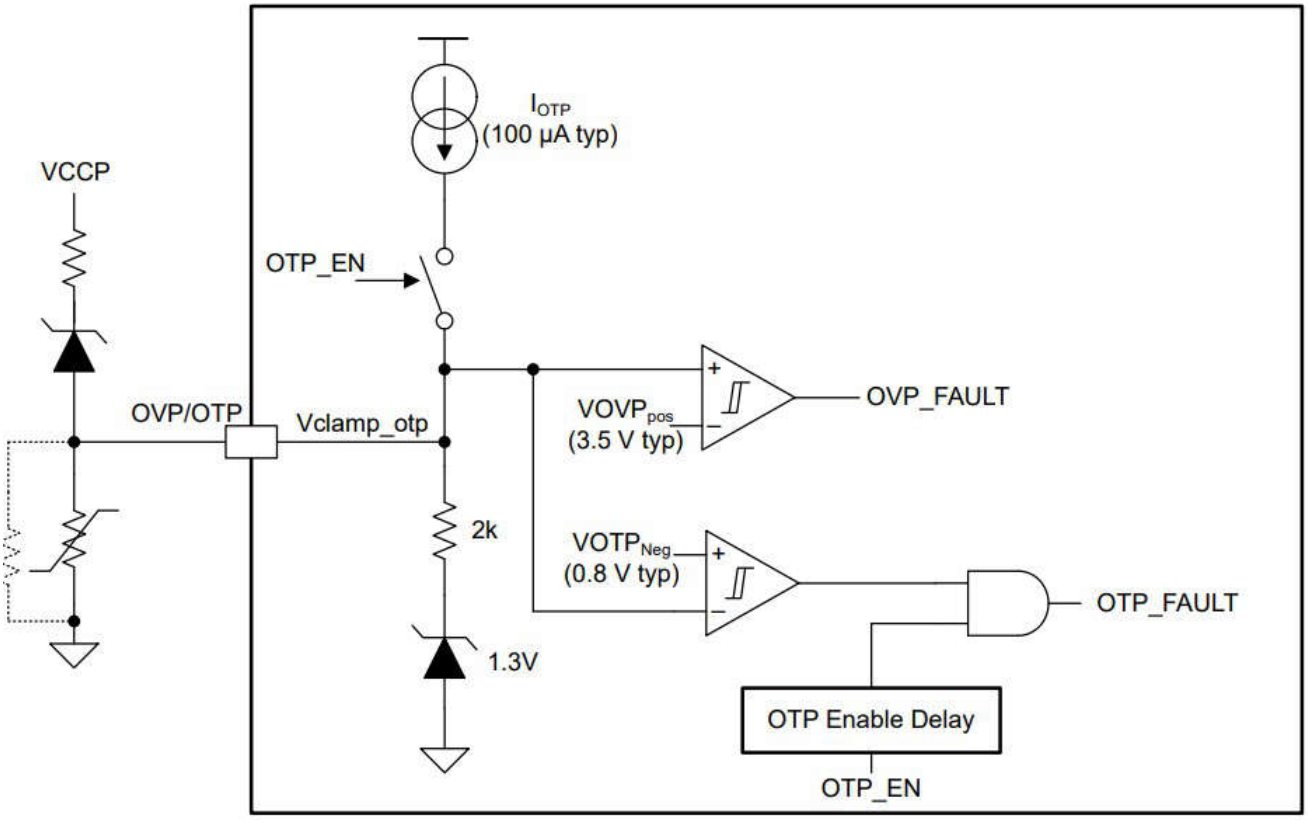

Figure 1-8. OVP/OTP Pin Architecture

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1.6 How to Set Up The TSET Pin in UCC25661x Family?

At the startup of the controller, TSETA and TSETB voltages are programmed. V_{TSETB} voltage configures the minimum frequency for IPPC operation and the maximum dead time. Whereas, (V_{TSETA} – V_{TSETB}) configures the integrator time constants that help to set the FBReplica magnitude for a given power output. So, while selecting TSET, first check what is the minimum switching frequency of the converter at full load and select a TSET option from the TSET table so that the minimum switching frequency at that TSET option is less than the minimum switching frequency. After that, select another TSET option which sets the VCR synthesizer integrator time constants to make sure that Vfbreplica vs Pin graph remains in between 2 (At slight load) to 4V(at peak load). If Vfbreplica touches 4.5V, the controller hits overload protection (OLP) and conducts the overload current for 100ms and after that it goes to 1sec fault.

For example, suppose a converter has a minimum operating frequency of 350kHz, so a user can select any TSET option between one to 12 for TSETB. Then, suppose, upon checking Pin vs VfbReplica graph in the design calculator, the user can select any TSET option between seven to nine to make VfbReplica vs Pin graph within two to four . Then, for this case, the TSET option with higher integrator time constant is preferable (for example, TSET option seven). The reason is with the reduction in integrator time constant, the bandwidth of the system increases. Thus, with a large load transient, resonant current as well as ISNS voltage can rise more than OCP threshold level (3.5V) for some of the cycles momentarily and can reach a false OCP level. Figure 1-9 shows a snapshot from the design calculator for TSET selection in the previous example.

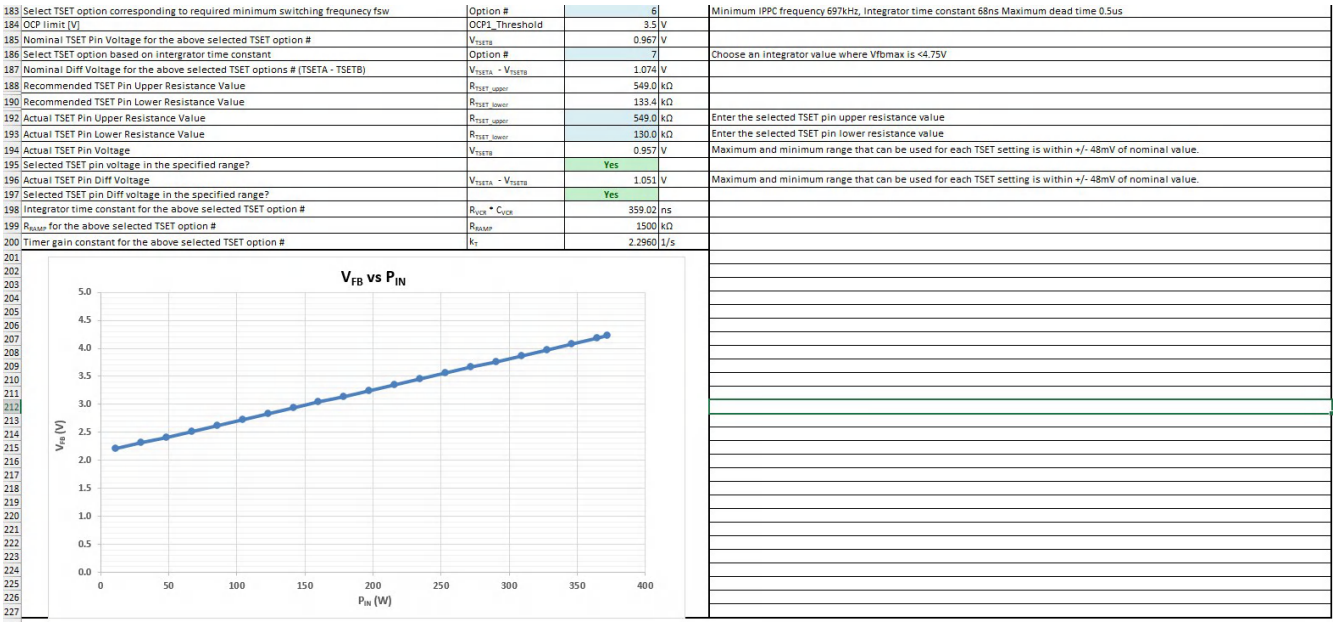

Figure 1-9. TSET Option Selection in Design Calculator

1.7 How to Avoid FB Pin Saturation? How to Detect it?

The FB pin of UCC25661x is current source driven. Thus, the FB pin voltage is normally constant (3.5V typically). If we want to check if the FB pin voltage is saturated or not, FB pin voltage must be checked. If the FB pin voltage drops below 3V, it indicates that the opto-coupler associated to the FB pin got saturated. If FB pin saturates, the transient response of the converter suffers. Avoid this by using the following circuit, adding a 1.5V Zener (D100) and 2.22k resistor (R100) between the V5P pin and the FB pin, as shown in Figure 1-10.

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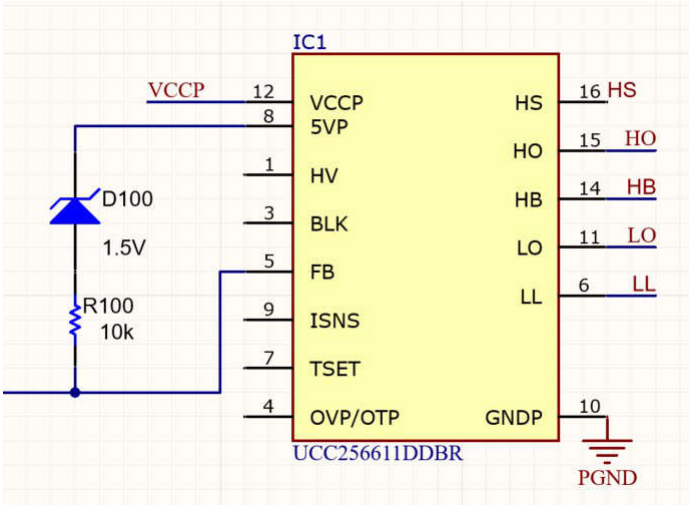

Figure 1-10. Circuit Implementation to Keep FB Pin Out of Saturation

1.8 Can the Device Sustain Damage if the HV Pin Current Goes Beyond What is Mentioned in the Datasheet?

The HV current is internally clamped to maximum 13.8mA. HV current cannot go beyond that. 1k-5k ohm HV resistors are recommended in the HV pin. if resistance in HV pin is increased too much, voltage drop across the resistor is higher and limits the minimum input voltage from where the IC can operate.

1.9 How does TON extension work in UCC25661?

During start-up and for the first few switching cycles, the MOSFET on the primary side can experience body diode reverse recovery and hard switching. The experience is mainly due to the fact that at start-up, the resonant capacitor can have DC bias voltage which is off from the steady state operating voltage of Vin/2 as shown in Figure 1-11 or zero resonant current at tank at the time of startup, as shown in Figure 1-12. These conditions lead to an asymmetry in the resonant tank current at start-up. In the first few cycles, asymmetry can be high enough that the current at the point of switch turn-off is in the wrong polarity. TON extension avoids the wrong polarity of current using UCC25661x device. Figure 1-11 and Figure 1-12 shows TON extension to fix the wrong polarity of current within early cycles.

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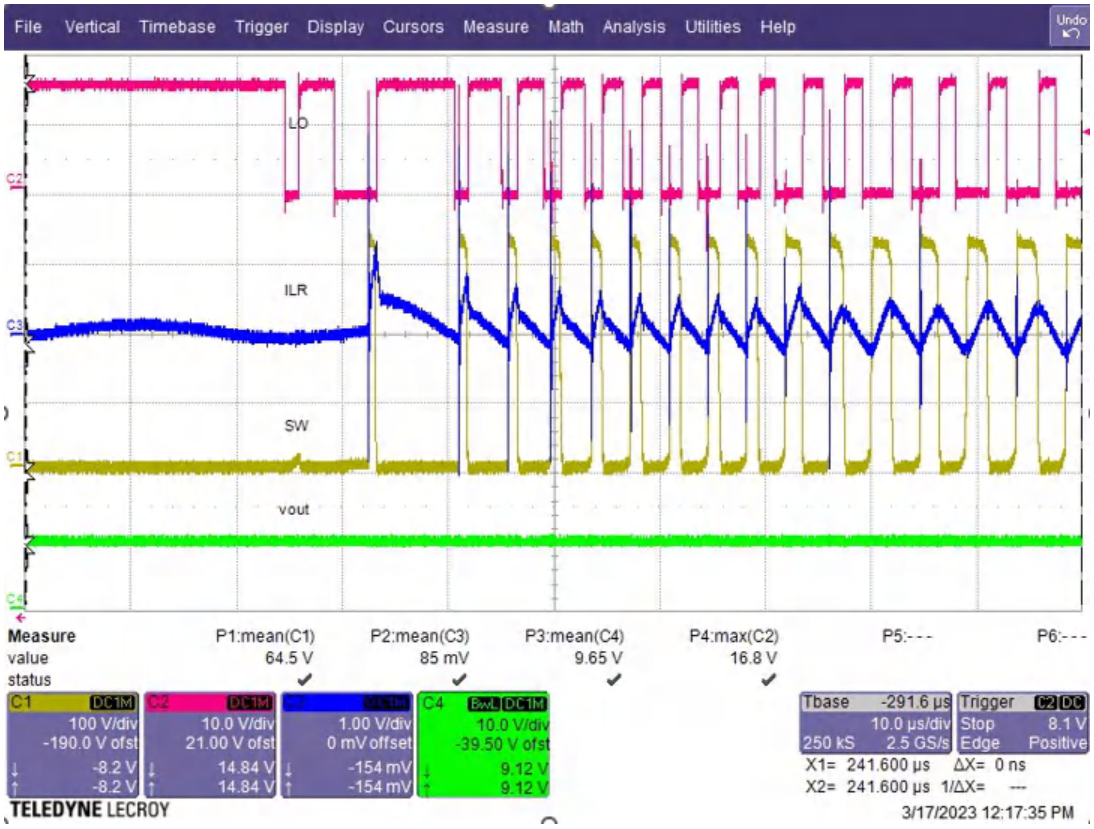

Figure 1-11. Startup Switching Waveform of UCC25661x

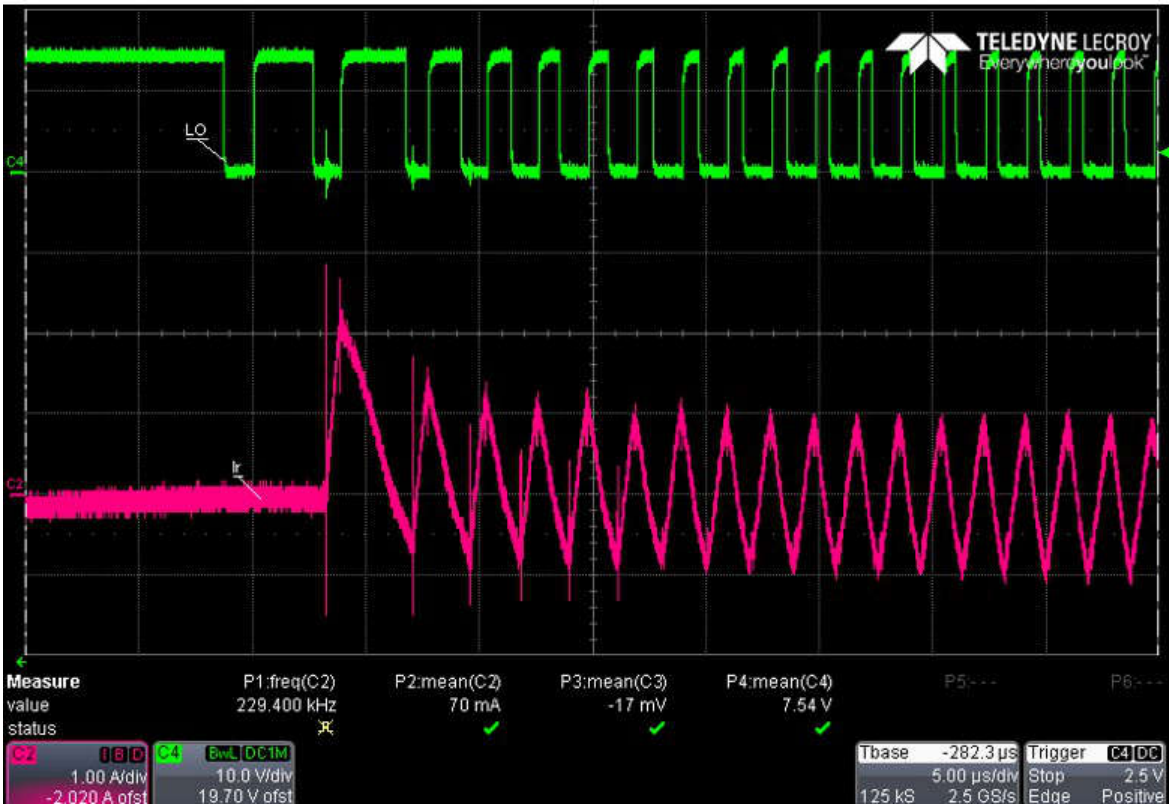

Figure 1-12. TON Extension in UCC25661x

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1.10 How ZCS Protection Works in UCC25661x?

ZCS typically happens when the LLC operates at heavy load condition and the switching frequency is too low. ZCS detection relies on the resonant current polarity detection (IPolarity). The IPolarity comparator detects the direction of the resonant current. The capacitive region detection is done by checking the resonant current polarity at HSON or LSON falling edge. If the resonant current is positive at LSON falling edge, or negative at HSON falling edge, the ZCS signal in the waveform generator is turned high. When a ZCS event is detected, the internal soft start ramp voltage is slowly reduced. When the internal soft start ramps down, the switching frequency is also forced to increase, forcing the converter out of capacitive region. In the event of a persistent ZCS condition for a period of 10ms, the UCC25661x family controller ceases switching and move to the fault state.

When operation nears the inductive/capacitive boundary, the resonant current decreases before the gate is turned off. If the ISNS waveform is less than the VISNS_ZCS threshold, the gate pulse HO is terminated early instead of waiting for the VCR waveform to cross the VTH boundary. This early gate termination scheme is capable of leaving enough resonant current at the gate turn-off edge to drive the ZVS transition during the dead-time. Similar explanation holds good for the LO gate pulse.

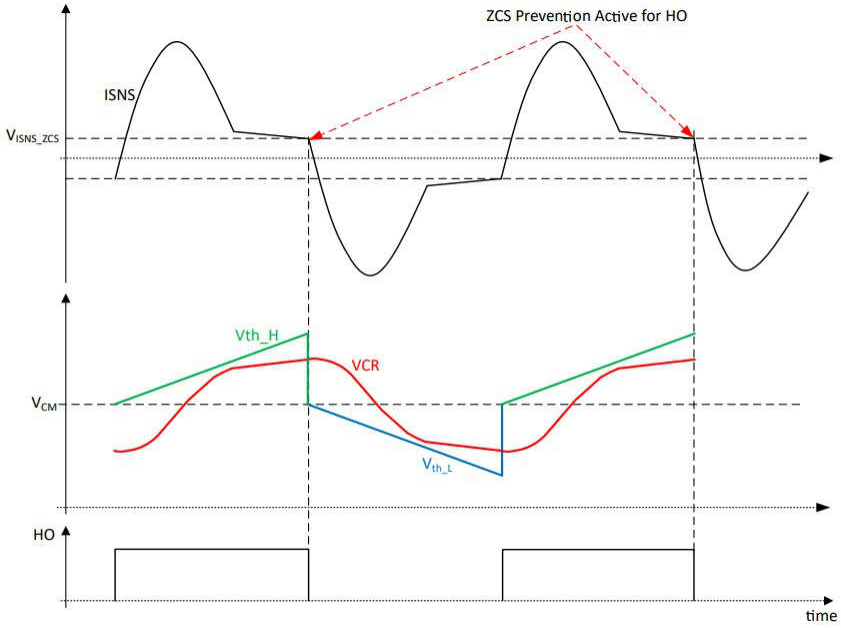

Figure 1-13. ZCS Avoidance Algorithm at ZCS Boundary

1.11 How does Adaptive Deadtime Work?

During the dead time, the HS node slews from one input rail to the other due to the inductive resonant current. To achieve zero voltage switching (ZVS) turn on, the dead time must be long enough for the resonant current to fully charge or discharge the HS node. After the body diode starts conducting, the MOSFET must be turned on quickly. Too long of a turn on delay can result in reverse resonant current and lead to the loss of ZVS. The voltage drop on the body diode is higher than that on the MOSFET channel. Optimized dead time can help to minimize the power loss. The resonant current flowing through the HS node during the dead time depends on the LLC resonant tank design and varies by operating frequency and output/input voltage ratio. Therefore, the optimized dead time varies widely with LLC operating conditions. UCC25661x includes an adaptive dead time control to automatically find the optimized dead time across the entire operating range. The device detects the change of slew rate of the HS node voltage. During a switching transition, the slew rate rises up first and then drops back to zero. A slew rate detector is used to detect the moment when the slew rate drops below a pre-defined threshold. A slew done event is only detected when the slew rate during dead time crosses the threshold and then drops back below the threshold. In burst mode, during a ZCS prevention operation or in power stages where the slew rate can be slow, the resonant tank current polarity signal (Ipolarity comparator output) is used to augment the slew rate detector. Taking advantage of the natural symmetric operation of LLC,

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the slew rate detector determines only the dead time between high-side switch turn off and low-side switch turn on. This dead time is copied and applied to the dead time between low-side MOSFET turn off and high-side MOSFET turn on.

There are a few exceptions where the dead time is not copied

1. Missing slew rate detector signal in the previous High to Low transition,
2. ZCS detection in the previous cycle

Under these conditions, the Ipolarity comparator based on the ISNS signal is used to adjust the dead time during low to high transitions.

1.12 How is the Dead Time in UCC25661x Determined During ZCS Detection and in the Absence of Valid Slew Rate Detection?

Case 1: Valid Slew Rate Detection and No ZCS

As soon as the high side gate (HO) is turned off, the low side gate (LO) is turned on after the slew rate is detected. The same dead time is copied over during low side turn off to high side turn on.

Case 2: No Slew Rate Detection and No ZCS

If no valid slew rate detection occurs after the HO turn off, the dead time during both transitions (HO turn off to LO turn on) and (LO turn off to HO turn on) depends on the resonant current polarity. Furthermore, this dead time does not exceed 1us or 0.5us, depending upon TSET settings.

Case 3: ZCS During HO Turn Off and No ZCS during LO Turn Off

If the ZCS is detected during HO turn off, the dead time from HO off to LO on is determined by polarity of the resonant current (IPolarity signal). The maximum dead time here does not exceed 1.1us. The dead time during LO turn off to HO turn on depends on the resonant current polarity. Furthermore, this dead time does not exceed 1.1us.

Case 4: No ZCS During HO Turn Off and ZCS during LO Turn Off

The dead time during HO off to LO on depends on the slew rate detection similar to case1. However, if no valid slew rate detection occurs after the HO turn off, the dead time during HO turn off to LO turn on depends on the resonant current polarity. Furthermore, this dead time does not exceed 1us or 0.5us, depending upon the TSET option. If the ZCS is detected during LO turn off, the time from LO off to HO on is determined by the polarity of the resonant current (ISNS signal). The maximum dead time here will not exceed 1.1us.

Case 5: ZCS During Both HO Turn Off and LO Turn Off

If the ZCS is detected during HO turn off, the dead time from HO off to LO on is determined by the polarity of the resonant current (IPolarity signal). The maximum dead time here does not exceed 1.1 us. If the ZCS is detected during LO turn off, the dead time from LO off to HO on is determined by the polarity of the resonant current (IPolarity signal). The maximum dead time here does not exceed 1.1us.

1.13 How to Test UCC25661 Without Applying High DC Voltage in Input of the Converter?

15V has to be applied to Vcc pin from an external DC source. 1.5V has to be applied at the BLK pin. LO and HS pin must be probed to check low side FET gate-source voltage and switch node voltage. In this condition, some LO pulses should come. Then, slowly increase the DC input voltage to 20V and in steps to 50V and check LO pulses and switch node. If this is correct, the BLK pin of the UCC25661 can be powered by input voltage and BLK resistors and high voltage can be applied at the input side of the converter.

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1.14 How to Connect GaN With UCC25661x?

UCC25661x can switch up to 750kHz. Therefore, it is simple to integrate the UCC25661x family to GaN devices. For example, if UCC25661x must be connected with LMG2650, then the connection is shown in Figure 1-14.

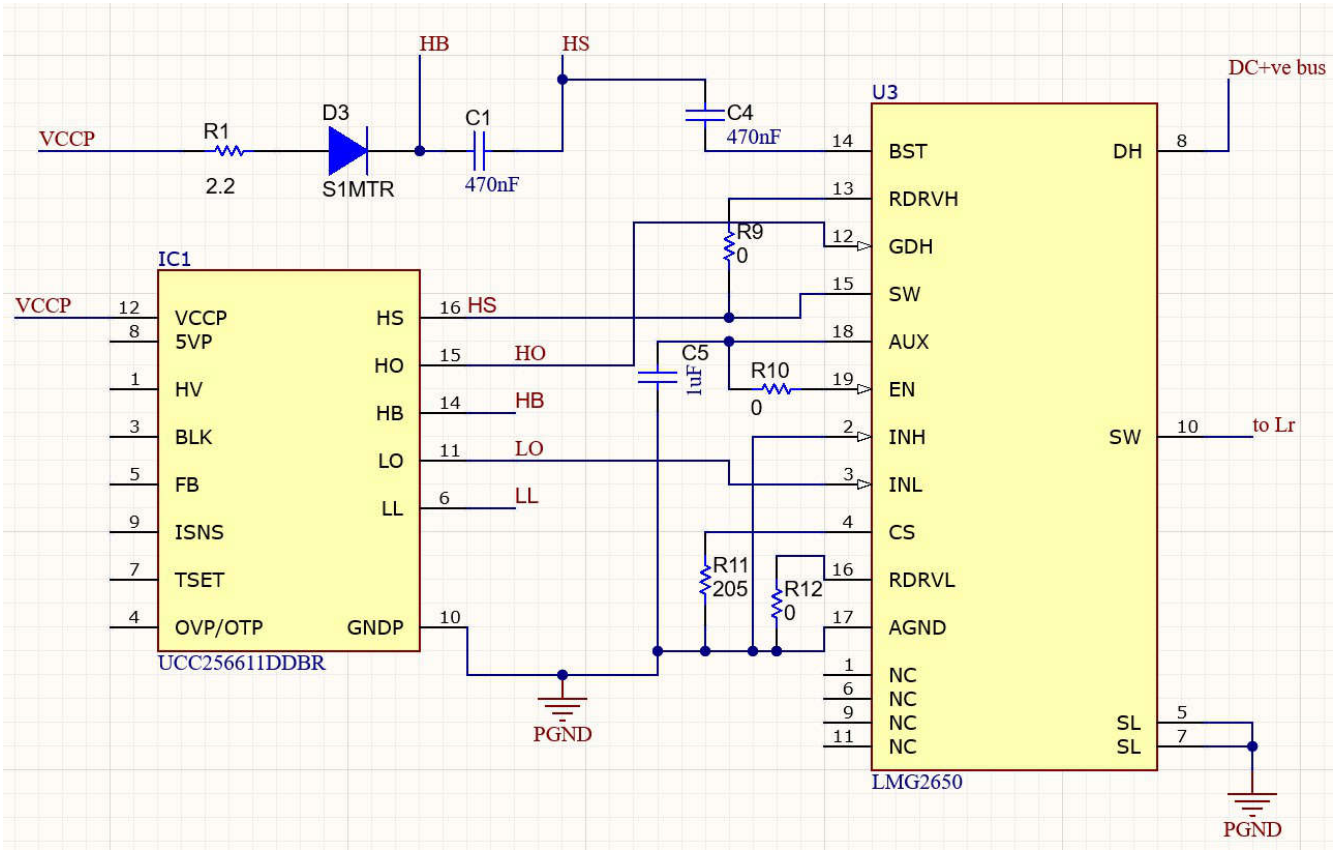

Figure 1-14. LMG2650 Interconnection With UCC25661x

1.15 How Much Maximum LL, TSET and ISNS Pin Decoupling Capacitors Must Be Used?

Generally, decoupling capacitor of not more than a value of time constant 0.5ms are recommended at the LL and TSET pin. Higher capacitance than the recommended values can cause increase in time constant at the respective pin, which can lead to wrong programming at respective pins while programming during startup. Maximum of 1nF decoupling capacitor is recommended at ISNS pin. LL, TSET and ISNS pin decoupling capacitors must be placed near the IC.

1.16 How Can Burst Mode Programming Be Changed While Running the Controller?

Dynamic LL pin configurations can be done at LL pin of UCC25661x, as shown in Figure 1-15 . R3 can be used as a parallel resistor to R2 by turning on Q1 with the help of the LL_Control signal and the PC1 opto-coupler. VLLA is programmed at the time of startup, whereas VLLB is sensed by the controller throughout the operation. Thus, VLLB can be changed by using resistor values of R1, R2 and R3. Also, to disable burst mode at any time of operation, R3 value must be chosen as 0Ω. If there is isolation required, the LL_Control signal can be applied to gate of Q1 w.r.t PGND directly.

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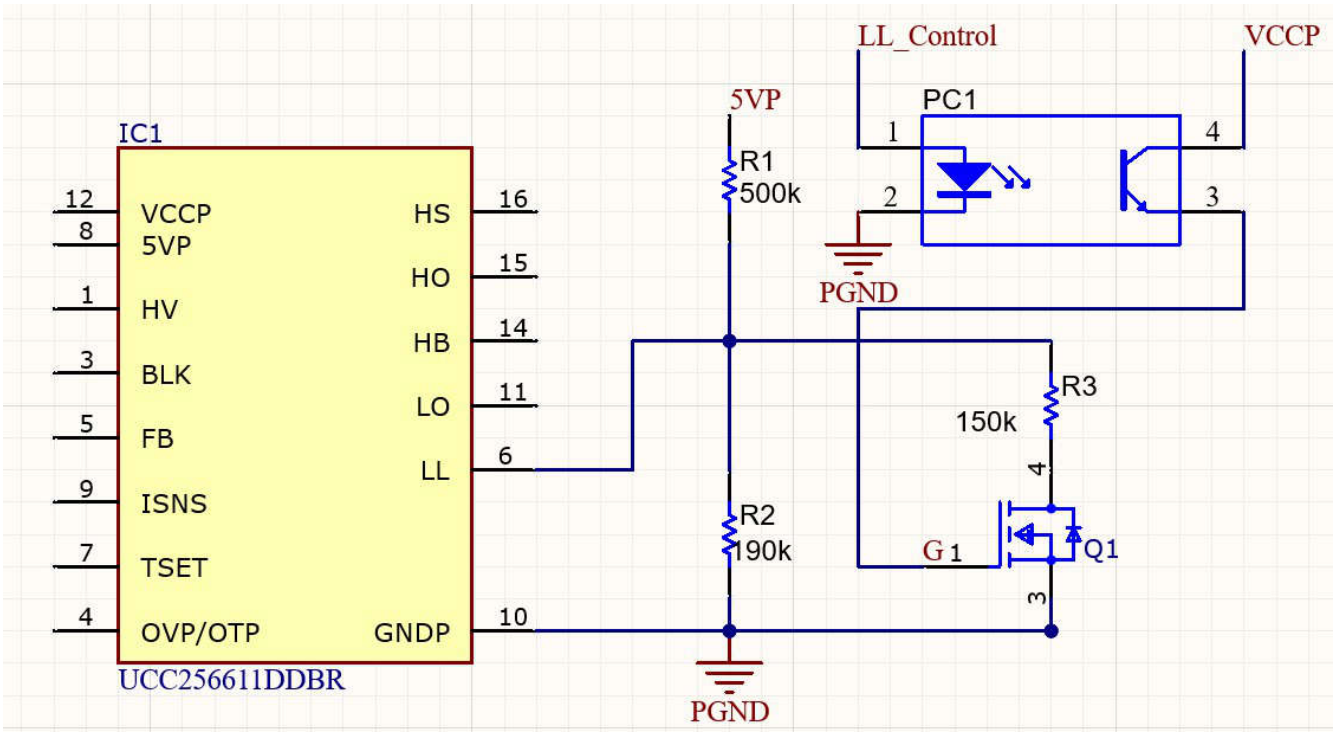

Figure 1-15. Dynamic LL Pin Circuit Diagram in UCC25661x

1.17 Summary

UCC25661x is an analog LLC controller that can switch up to 750kHz in normal conditions which allows it to integrate with GaN. The controller is configured according to the user. UCC256610 and UCC256614 variants within this family are capable of supporting wide input LLC applications.

1.18 References

1. Texas Instruments, *UCC25661*, product page.
2. Texas Instruments, *UCC25661-Q1*, product page.
3. Texas Instruments, *UCC25661x Design Calculator*, design calculator.
4. Texas Instruments, *UCC25661EVM-128*, EVM.

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